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N-Path Mixer with Wide Rejection Including the 7th Harmonic for Low Power Multi-Standard Receivers

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Outline

- Context: Multi-Standard Receivers
  - Principle of N-path Mixers
  - Principle of Harmonic Rejection N-Path Mixer
  - Introduction to HR-10PMeq
  - Measurement Results
  - Conclusion and Perspectives
Evolution of Cellular Networks

Mandatory to use:
Multi-standard receivers
Context of Multi-Standard Receivers

Main requirements:
- Low power consumption
  - Technology level
  - “Protocol” communication level
  - Architecture level
- Wide band transceiver

**General Purpose of this work:** Introduce a novel design of a wideband architecture N-path receiver with low power consumption and less complexity

**Solution:** *N-path Receiver*

- Power and size 😊
- Tunability 😊
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N-Path Mixer

\[ V_{Cn}(t) = V_{RF}(t) \cdot eflo(t) \]

\[ eflo(t) = S_n \text{ for path } n \]

\[ T_{LO} = 1/f_{LO} \]

\[ EFLO(Nf_{LO}) = 0 \]
Frequency Transposition Principle and Issues

1. Desired channel
   - $f_{RF}$
   - $f_{LO}$
   - $f_{IF}$

   Image of the RF signal w.r.t $f_{LO}$

   - $f_{RF}$
   - $f_{LO}$
   - $f_{RF_image}$

   Blocking / interfering due to the image

   Image filter before mixing

2. Jammer signal
   - $f_{RF}$
   - $f_{LO}$
   - $2f_{LO}$

   Blocking / interfering due to the jammer

   - $f_{IF}$

   ! Same issue for all the LO harmonics
Solution 1: Differential N-Path Mixer

Even Harmonics Rejection
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Harmonic Rejection N-Path Mixer: HR-NPM

Typical case: $H=N$

$H$ Gain Stages, $G_h$ is defined for $1 \leq h \leq H$; $G_h = \frac{\sin\left(\frac{2\pi}{H} (h)\right)}{\sin\left(\frac{2\pi}{H}\right)}$

$eflo(t) = \sum_{h=-\infty}^{+\infty} G_h \cdot \delta(t - hT_s) \ast g(t)$

$T_s = T_{LO}/H$ then $F_s = F_{LO} \cdot H$

$|EFLO(f)| = \frac{A}{2} \cdot \text{sinc}(\pi T_s f) \sum_{n=0}^{+\infty} \delta(f - n \cdot F_s \pm F_{LO})$

$F_s = \frac{F_{LO}}{H}$ then $F_s = F_{LO}$. $H$

$G(f)$

$\text{first non-rejected harmonic}$

@ $(H-1) F_{LO}$
Example: Conventional HR-8PM

- \( N=8 \)
- \( H=8 \) with 2 switches connected to \( G=0 \)

1st non-rejected harmonic @ \( N-1 \)

- 1st
- 7th
- 9th
Conventional HR-NPMs vs New Architecture

First non-rejected Harmonic Order

Harmonic Rejection Band

Power Consumption

Nb of LNA gains

Conventional HR-NPMs

Implemented HR-10PMeq

Nb of switches

HR-6PM

HR-8PM

HR-10PM

HR-12PM

24

48

40

80

120

5

7

9

11
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$\pi$-Delayed HR-10PM

H=10 with 4 switches connected to G=0
\( \pi \)-Delayed HR-10PM: Overlapping Issue

\[ HRR5 = 10\text{dB} \]

\[ HRR5 = 20\text{dB} \]
Modified π-delayed HR-10PM: HR-10PMeq

H=10 with 2 switches connected to G=0

NO OVERLAPPING CLOCKS
HR-10PMeq: Block-Circuit-PCB design
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HR-10PMeq: Measurement Results

Input Return Loss $S_{11}$:

- Circuit is matched for the targeted frequency band 0.17-1.2GHz: $S_{11}<-15\text{dB}$

Conversion Gain $G_c$:

- $G_{c\text{max}} = 13\text{dB}$
  - @ IF = 5MHz

3rd order Intercept Point:

- In-band IIP3 = -3.5dBm
## State of the Art

**excluding transimpedance amplifiers TIA, ***Including TIA necessary for harmonics rejection**

<table>
<thead>
<tr>
<th>RX</th>
<th>Frequency (GHz)</th>
<th>NF (dB)</th>
<th>Gc (dB)</th>
<th>Pdc (mW)</th>
<th>IN-IIP3 (dBm)</th>
<th>HRR$_{3,5}$ (dB)</th>
<th>CMOS Tech. node</th>
</tr>
</thead>
<tbody>
<tr>
<td>[1] LNA+HRNPM+Gm+Harmonic Recombination</td>
<td>0.2-1</td>
<td>5.4-6</td>
<td>36</td>
<td>30**</td>
<td>NA</td>
<td>51-52</td>
<td>65nm</td>
</tr>
<tr>
<td>[2] LNA+mixer+divider</td>
<td>0.4-0.9</td>
<td>4</td>
<td>34</td>
<td>40***</td>
<td>3.5</td>
<td>60-64</td>
<td>65nm</td>
</tr>
<tr>
<td>[3] LNA with current Reuse RF front End+Feed forward passive mixer</td>
<td>0.15-0.85</td>
<td>4.6±0.9</td>
<td>51±1</td>
<td>10.6-16.2</td>
<td>-12</td>
<td>53-51</td>
<td>65nm</td>
</tr>
<tr>
<td>[4] LNA+8PM</td>
<td>3-6</td>
<td>3</td>
<td>58</td>
<td>35</td>
<td>NA</td>
<td>N/A</td>
<td>28nm</td>
</tr>
<tr>
<td><strong>This work</strong></td>
<td>0.17-1.2</td>
<td>13.3</td>
<td>13</td>
<td>22</td>
<td>-3.5</td>
<td>46-48</td>
<td>FDSOI 28nm</td>
</tr>
</tbody>
</table>
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Conclusion

• The proposed architecture is fabricated in 28nm FDSOI technology
  • 3 gains (Gain ratio=1.62)
  • 5 paths
  • 10 clock phases with duty cycle 1/10

  ➢ 1st harmonic @ 9th order
  ➢ HRR3, 5, 7 > 45 dB (measured for FLO = 300MHz)
  ➢ Power consumption of 22mW
  ➢ Frequency band: 0.17-1.2GHz
Perspectives

Power Consumption vs Nb of LNA gains

First non-rejected Harmonic Order

Harmonic Rejection Band

- Conventional HR-NPMs
- Implemented HR-10PMeq
- In progress

Nb of switches

- HR-6PM: 24
- HR-8PM: 48
- HR-10PM: 80
- HR-12PM: 120

In progress
References


THANK YOU!