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An Independent Dynamic Dead-Time Control for Reliable High-Voltage High-Frequency Half-Bridge Converters

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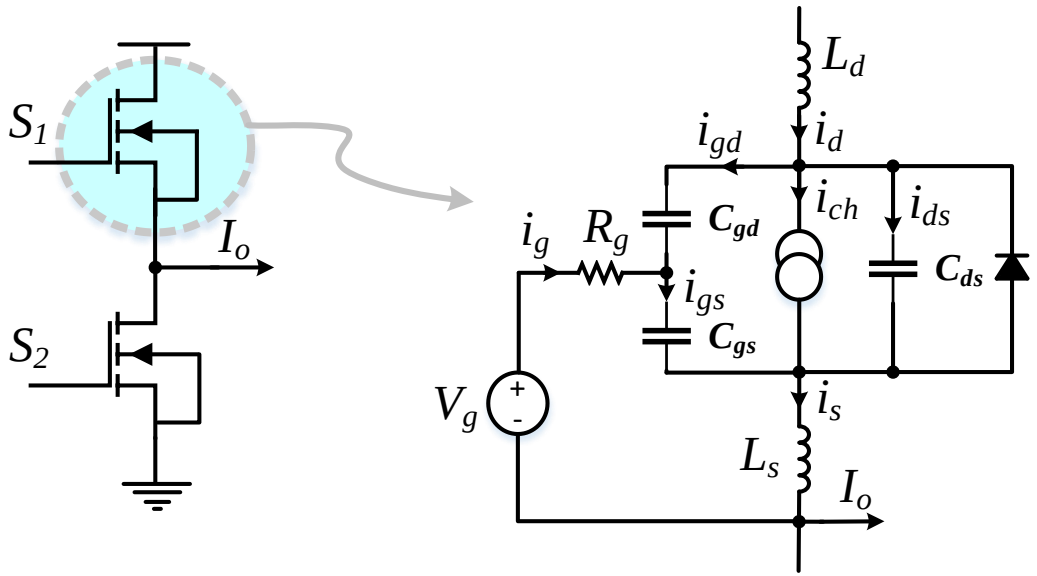
Outline

- Introduction
- Proposed dead-time circuit
- Circuit implementation
- Measured performance
- Validation with half-bridge circuit
- Power loss analysis
- Conclusion

An Independent Dynamic Dead-Time Control for Reliable High-Voltage High-Frequency Half-Bridge Converters

Introduction

- Different applications, require various types of power converters.
- DC–DC boost/buck converters, class-D power amplifiers, half-bridge converters.
- Applications: automation, wireless power transmission, and neural stimulations.
- Switching losses, conduction and gate charge losses; affect efficiency of power converter.
- Drawbacks, attributed to the parasitic inductances and capacitances of power switches.
- Accelerate the charge/discharge of C_{iss} , C_{oss}, mitigate switching and gate charge losses.



$$C_{iss}=C_{gs}+C_{gd}$$

$$C_{oss}=C_{gd}+C_{ds}$$

$$C_{rss}=C_{gd}$$

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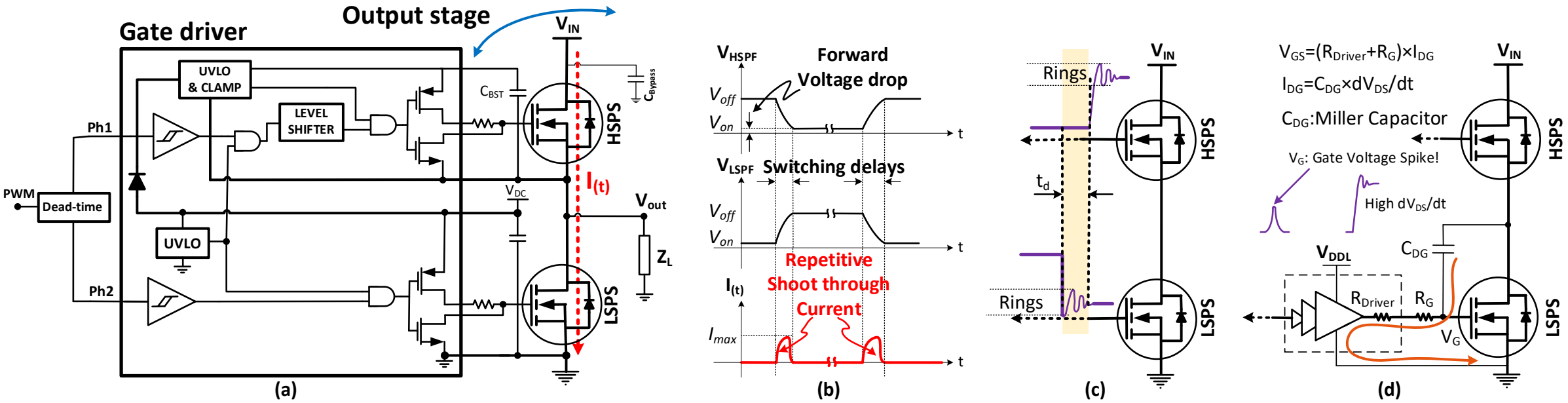
Introduction

- (a): Half-bridge convertor, dead-time part, gate driver, HSPS, LSPS.
- (b): One of complementary switches, turned on before the other switch turned off.
- (b): Shoot-through current, flow from the supply to the ground during the overlap time.
- (c) Shoot-through may also result from ringing in the driving circuit.
- (d) Formation of Miller capacitance at the gate of the low-side complementary switch.
- This condition results in the V_{GS} of the switches to exceed V_{TH}.



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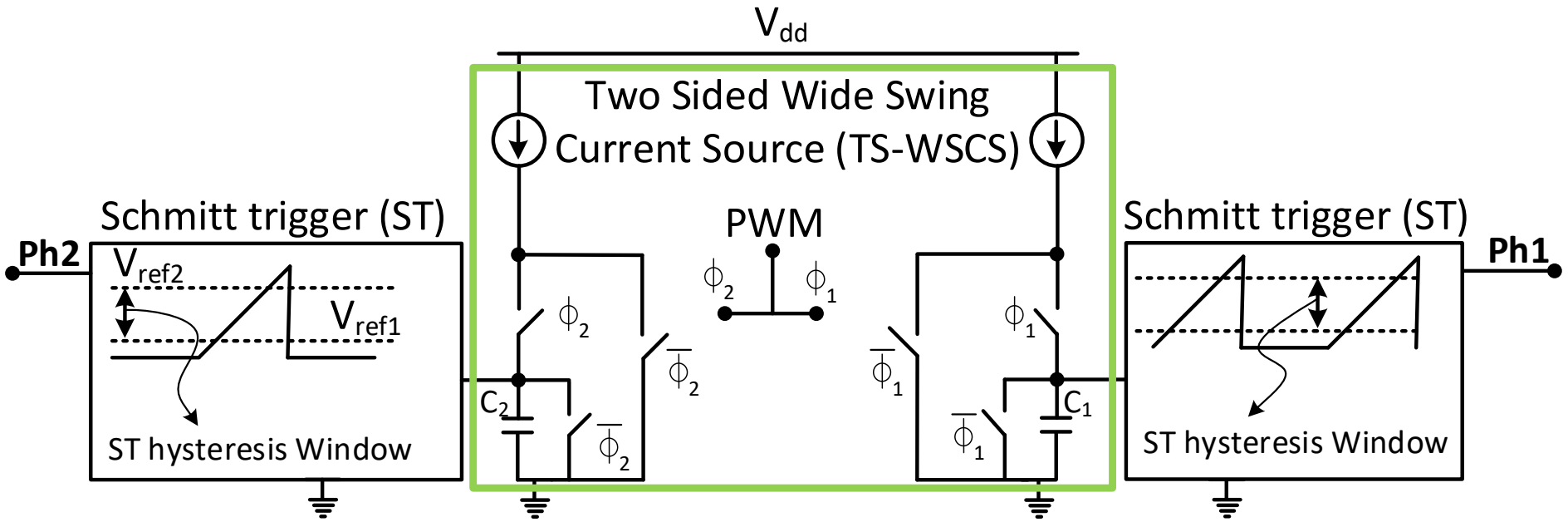
Proposed dead-time circuit

- Conventional dead-time circuits, cross-connected logic gates, generates p-second delays
- High voltage power converters, required longer delays, range of nano-second.
- Proposed dead-time circuit: TS-WSCS, 2 capacitors, three switches, two Schmitt trigger.
- Nanosecond delays, generate, mitigates shoot-through at the same time.
- Overall power losses in power converters, decrease.



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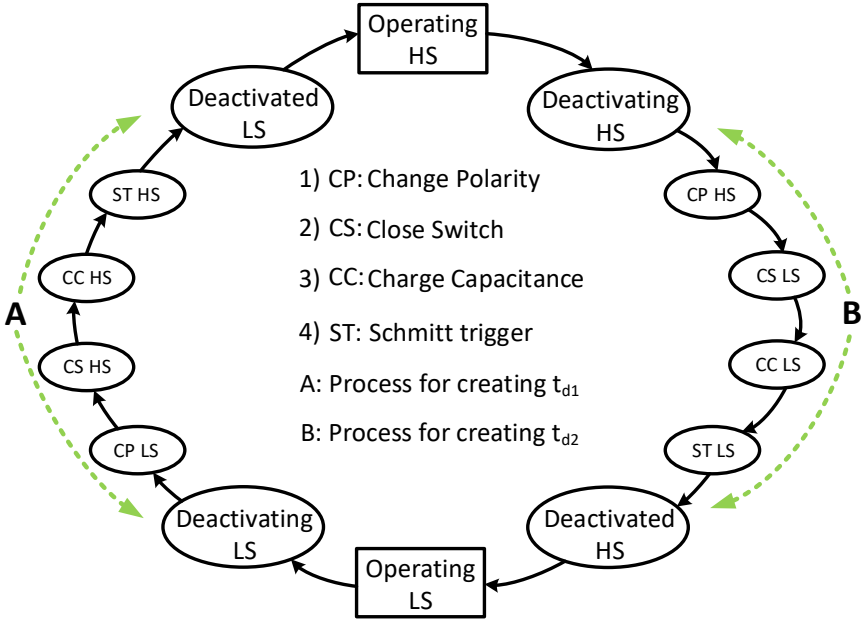
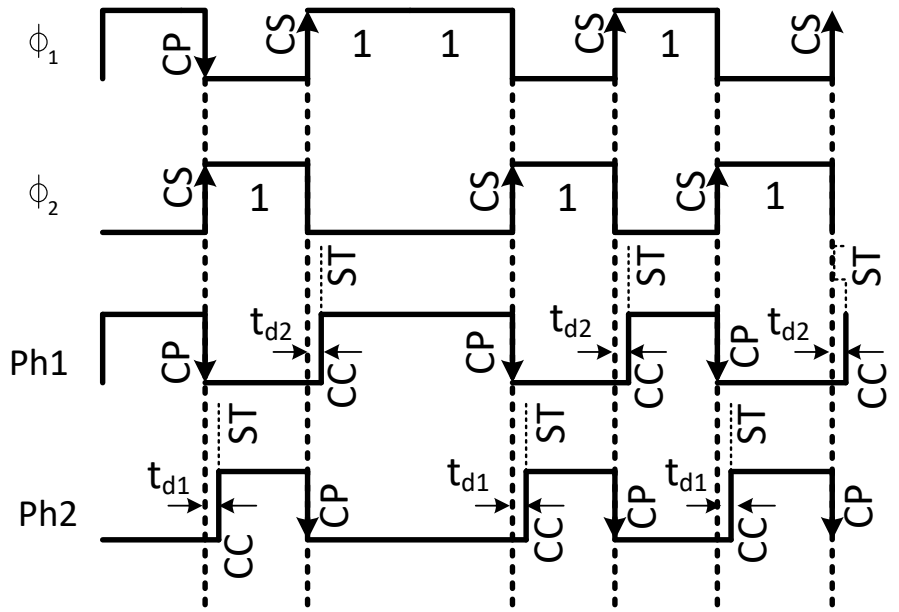
Proposed dead-time circuit

- Predefined state machine, reflects the originality.
- States in the finite machine, “CP”, “CS”, “CC”, and “ST”.
- Process “A” and “B”, time required, completely deactivate one power switch before the activation of the complimentary power switch.
- Timing diagram, includes four curves tagged by t_{d1}, t_{d2} and the different working states.





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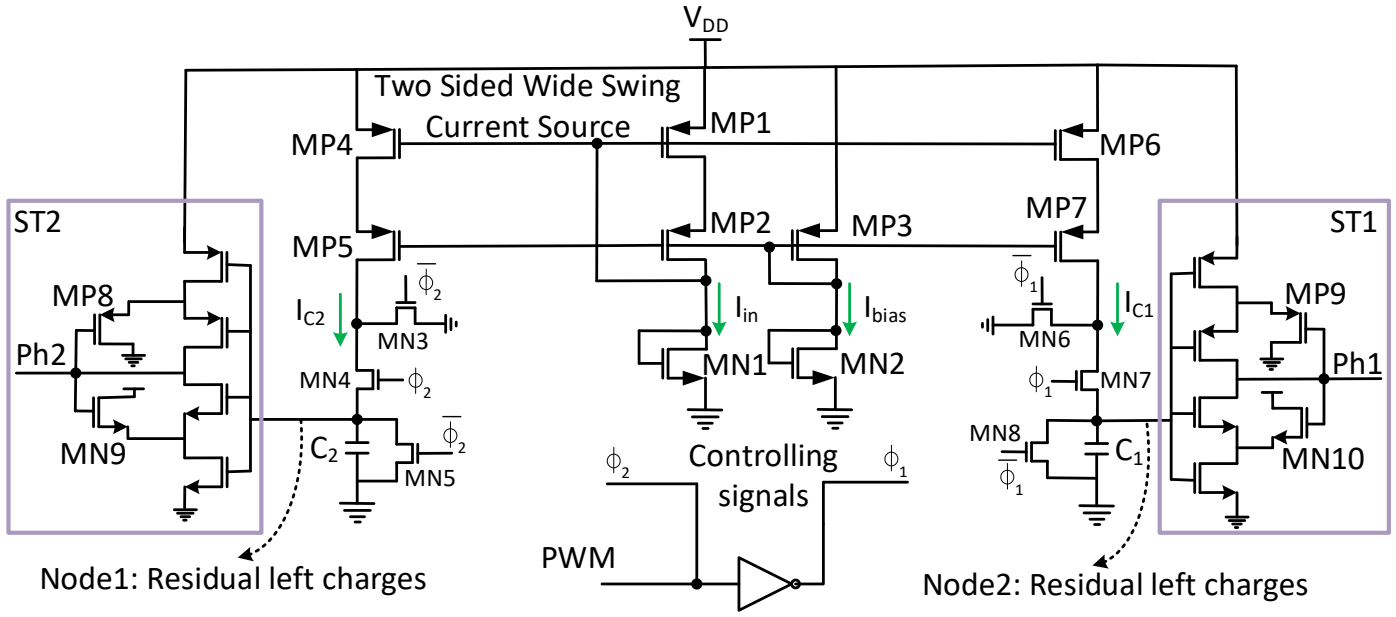
Circuit implementation

- Transistor-level implementation of the proposed dead-time circuit.
- Provide high-side and low-side delays of 35-ns and 62-ns to such a half-bridge converter.
- TS-WSCS supplies the charging current of capacitors C_1 and C_2.
- Diode connected transistors, current sources for respectively generating I_{in} and I_{bias}.
- Ramp signal, generated using the timing elements MN3-MN8, C_1-C_2, Φ_1-Φ_2.
- Schmitt triggers, reshape the ramp to a non-overlapping signals, Ph1 and Ph2.



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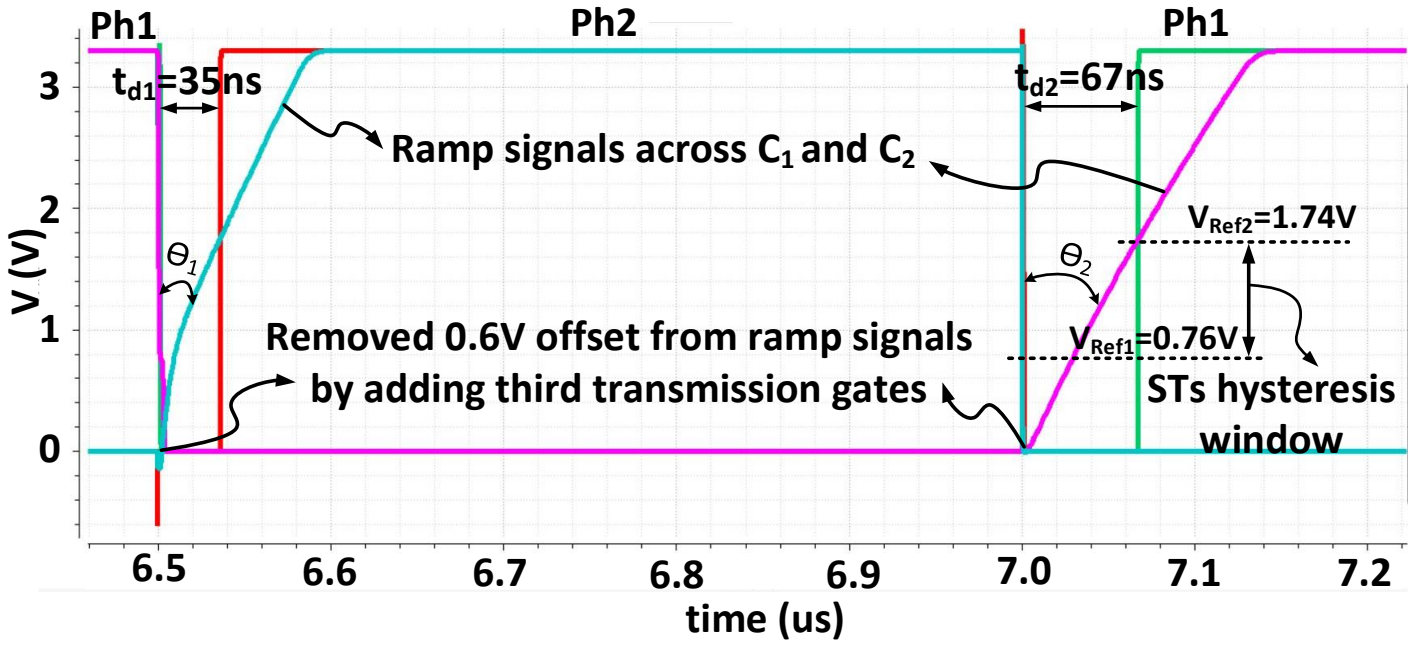
Circuit implementation

- Post-layout simulation; Ph1, Ph2, the ramp signal across capacitors (C_1 and C_2).
- Generated delays between the Ph1 and Ph2, rely mainly on the slope of the ramp signals.
- Capacitance of C_2, relatively large, the slope of the ramp signals, slow.
- Upper bound, ST on the corresponding side of C_2 meets the ramp signals later, $t_{d2}>t_{d1}$.



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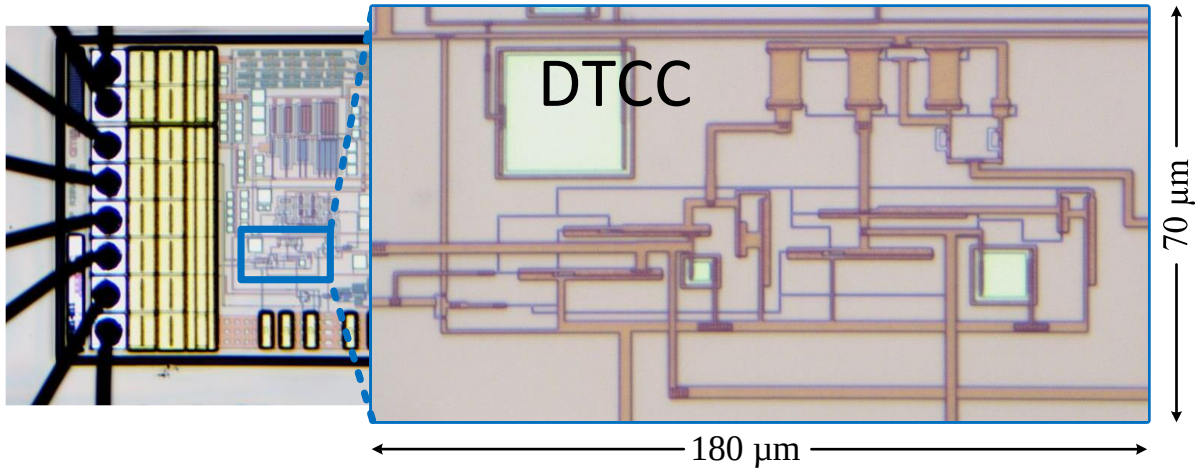
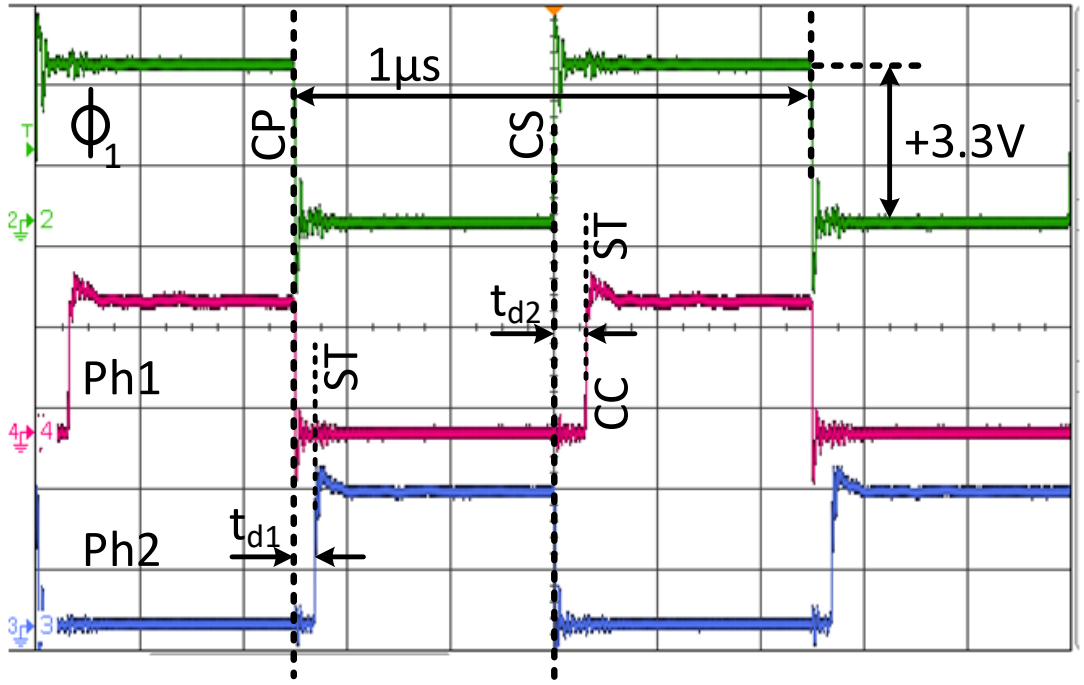
Measured performance

- The micrograph of the integrated chip prototype.
- The measured non-overlapping signals produced by the dead-time circuit prototype.
- Reached a good agreement between the experimental results and the projected timing dia.
- Four operating states, CP, CS, CC, ST, t_{d1}, t_{d2}.





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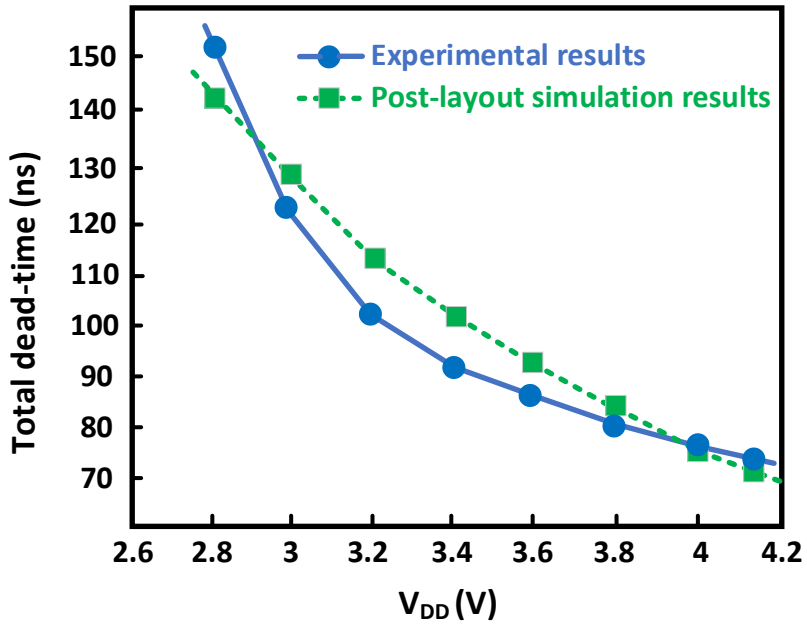
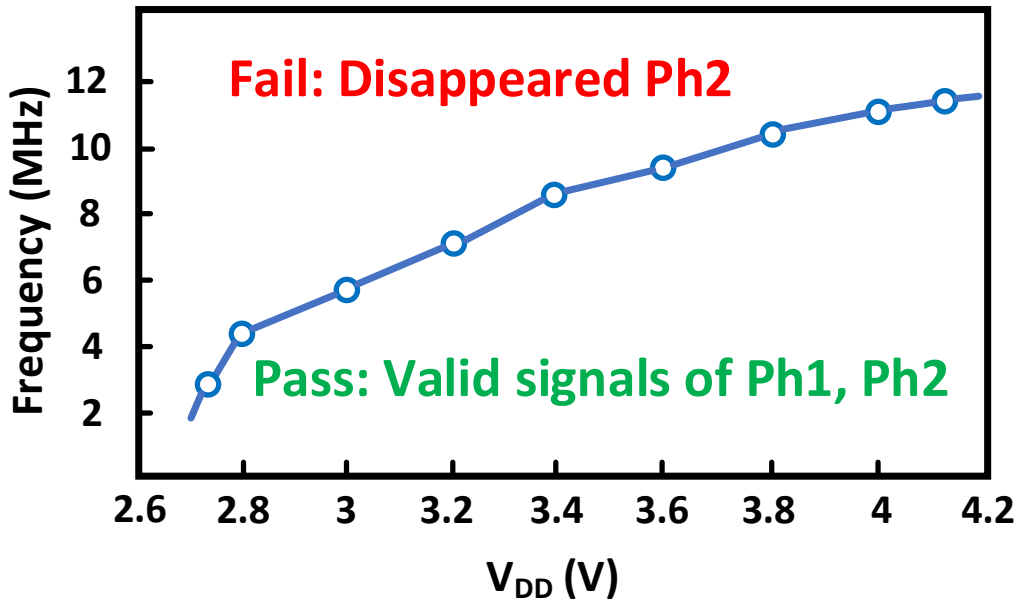
Measured performance

- Comparison of the experimental and post-layout simulation results.
- Dead-time delays variation versus the power supply voltage V_{DD}.
- An increase in the V_{DD} causes a decrease in the generated dead-time.
- Effect of V_{DD} on the maximum operating frequency of dead-time circuit.





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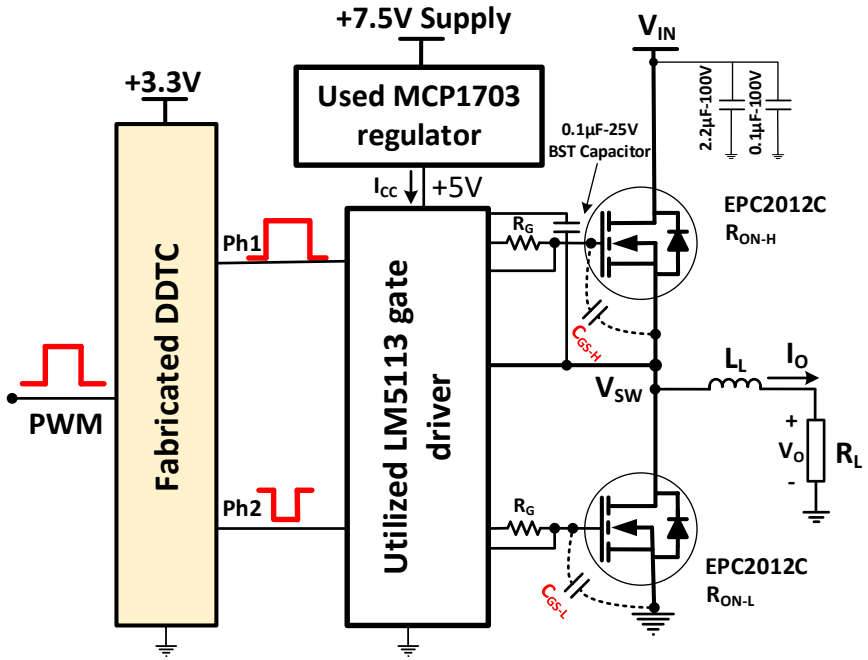
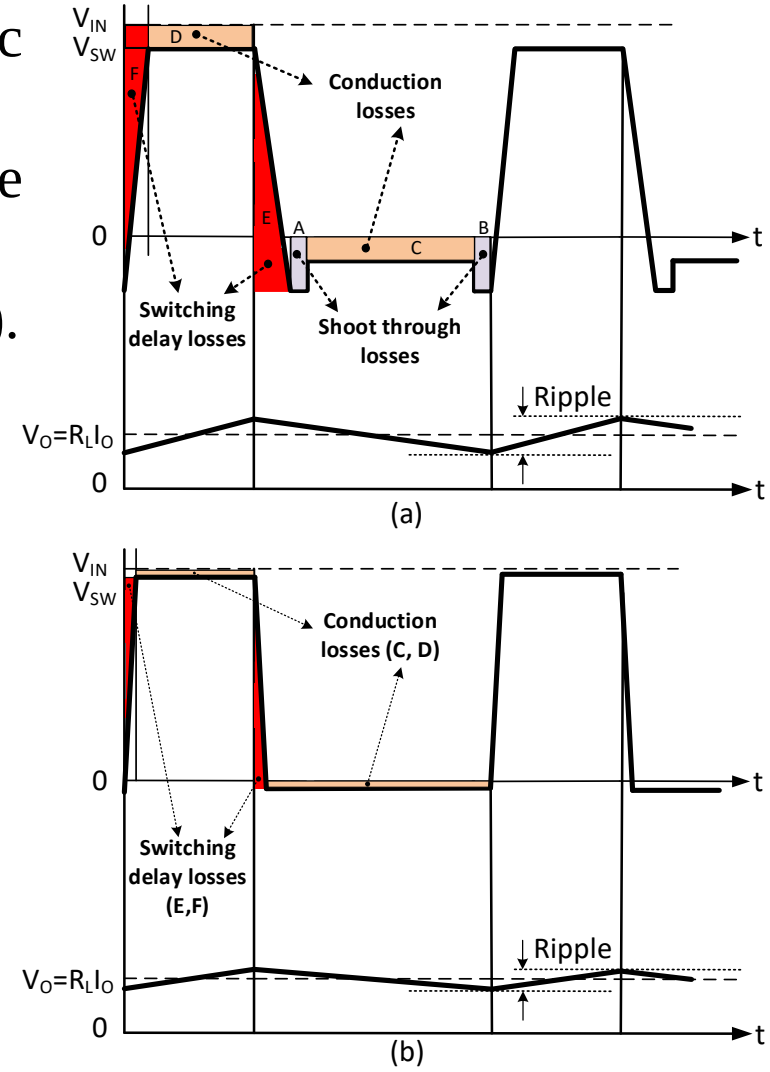
Validation with half-bridge circuit

- Validated the dead-time prototype by implementing a half-bridge c ircuit with commercial components.
- Shown the basic operations of the half-bridge circuit with inconve nient and convenient dead-time, parts (a) and (b), respectively.
- Highlighted the dead-time dependent losses (A, B, C, D, E, and F).





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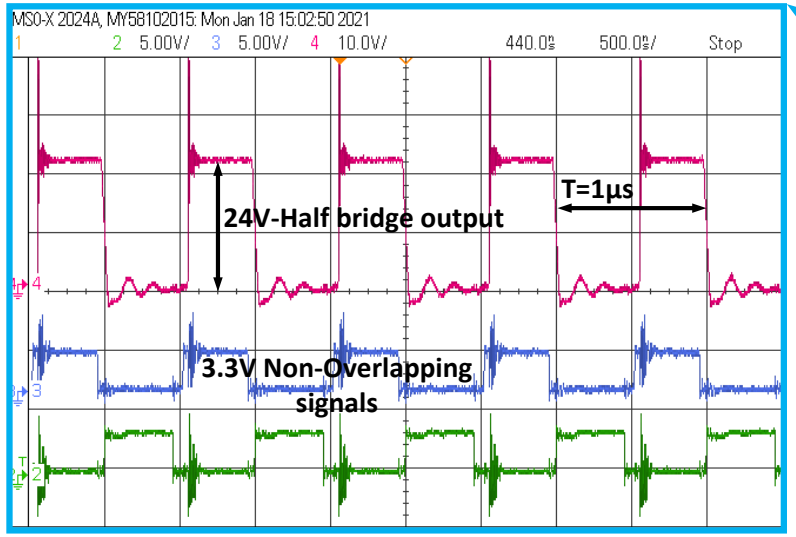
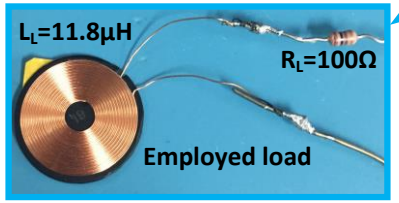
Validation with half-bridge circuit

- Experimental setup for characterizing the implemented half-bridge with the dead-time circuit.
- Size of the custom PCB used to characterize the half-bridge: 2.54 cm×3 cm.
- Size of power switches (5A, 200V): 1.7 mm × 0.9 mm.

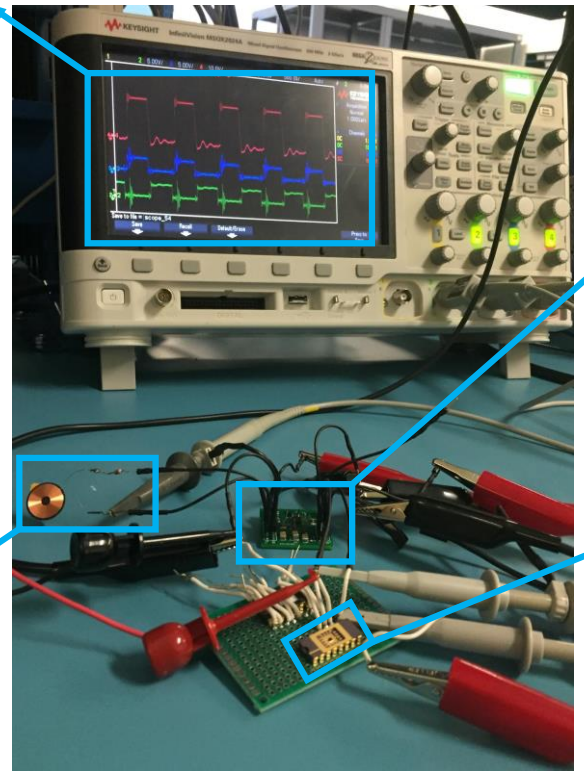


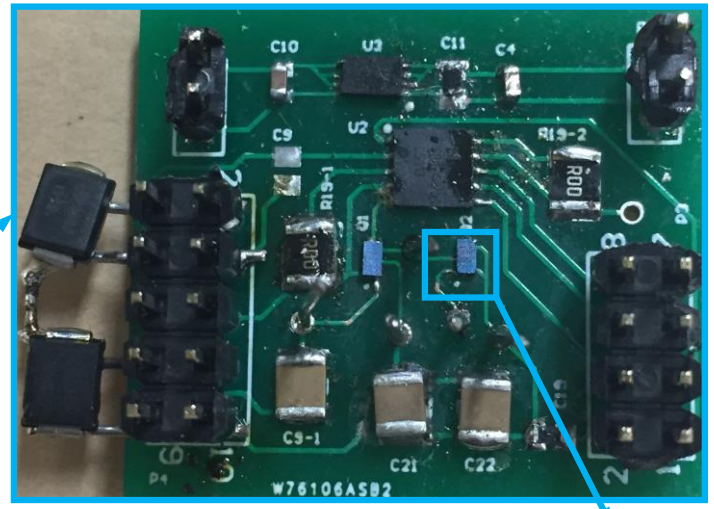
(a)

(b)

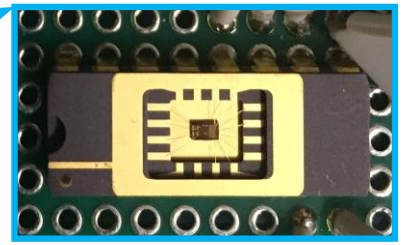


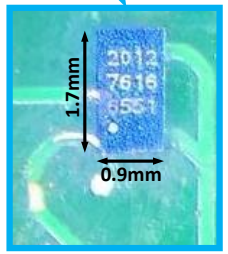
(c)


(d)



(e)


(f)



(g)

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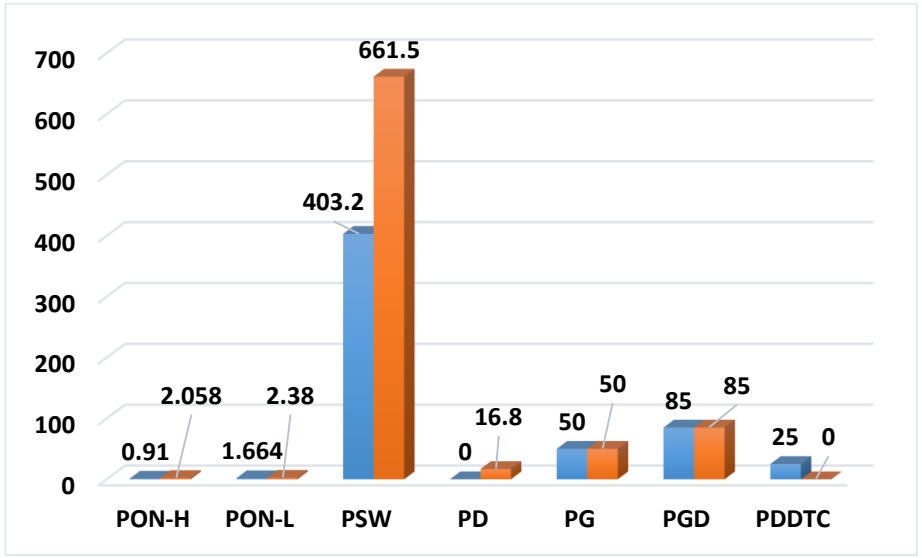
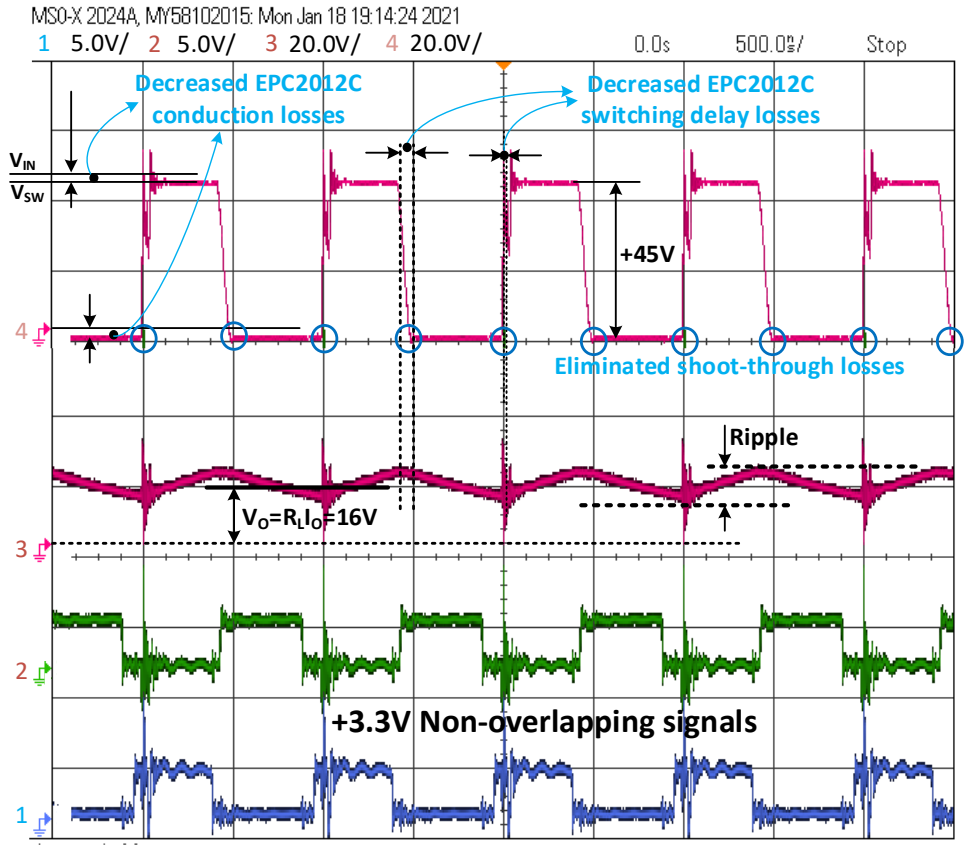
Power loss analysis

- Measured waveforms of the half-bridge with dead-time circuit, V_{IN}=45V, load: 100Ω, L=150μH.
- Dead-time dependent losses decrease significantly.
- P_{loss}=404.11mW without proposed dead-time circuit.
- P_{loss} = 663.558mW with proposed dead-time circuit.
- T_{Ja}=404.11mW×85°C/W+85°C=119.3°C.
- T_{Jb}=663.558mW×85°C/W+85°C=141.4°C.



Power Loss Distribution of Half-bridge



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Conclusion

- Switching frequency (f_p), dead-time delay (t_d), output current (I_O), input voltage (V_{IN}),
- Technology (Tech.), total loss improvement (ΔP_{loss}), and efficiency.
- Compared with the reported measurement results of other solutions.
- Dead-time circuit; produce relatively long and indep. time delays for power converters.
- Implemented circuit improves the dead-time dependent converter losses by 40%.

	[42]	[48]	[51]	[52]	**This work**
Results	Meas.	Meas.	Meas.	Meas.	**Meas.**
Tech.(nm)	180	65	350	350	**350**
f_p (MHz)	10	10	10	0.1	**1**
t_d (ns)	0.125	1	Analog	200	**35 and 62**
I_O (mA)	200	120	600	500	**210**
V_{IN} (V)	12	5	3.6	250	**45**
ΔP_{loss} (%)	30.5	--	--	--	**32**
Effic.	81.2%	76.4%	--	77%@20W	**82%**

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Question

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