A Monolithic GaN Power Stage with Low Propagation Delay and High Reliability Level Shifting for High Frequency Power Converter

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Abstract—In this article, a monolithic gallium nitride (GaN)-based half-bridge power stage is proposed for high frequency power converter. A level shifting technique with buffering device and shielding capacitance is designed to perform communications in half-bridge topologies with high reliability and low propagation delay. To prevent the missing pulse or output latch during deadtime, a negative voltage pull-down circuit is designed. Implemented with a 0.25µm 15-V enhanced mode GaN (eGaN) process, this work consists of optimized delay matching, monolithic gate drivers and power high electron mobility transistors (HEMTs) as well. The implementation results show that this work can achieve a propagation delay of no more than 6.5ns, a delay mismatch within 2.5ns and a CMTI capability above 150V/ns at 30Mhz switching frequency.

Index Terms—Monolithically GaN power stage, half-bridge, high frequency power converter, low propagation delay, high communication reliability, level shifting

I. Introduction

In recent years, gallium nitride (GaN) high electron mobility transistors (HEMTs) have aroused much concern in modern communication systems and automobile applications. The admirable figure of merit (FOM) of GaN HEMTs allow a GaN-based power converter operating at greatly higher switching frequency $f_{SW}$ than a silicon-based one [1], [2]. High $f_{SW}$ operation contributes to lower system volume and higher power density [3], [4], especially in the envelope tracking systems which require intensive switching for wider modulation bandwidths [5]–[7].

The low parasitic properties make monolithic GaN solutions stand out from their discrete device competitors, providing with better efficiency, reliability and performance in the higher switching frequency applications [8]–[10]. To best solve the trade-off between output voltage level, speed, and power consumption in monolithic GaN design without P-type GaN devices, the inverter and driver with bootstrap circuit have been extensively studied [11], [12]. In addition, these monolithic solutions also show a potential to deal with self-turn-off and electromagnetic interference (EMI) problems [13], [14].

However, most studies of monolithic GaN solutions have focused on single-channel driving, the monolithic half-bridge topology, which is more critical for power converters, has not been sufficiently studied. In [14], [15], some simple level shifters are designed, but these works lack a detailed discussion in terms of trade-offs and fault scenarios. Thus a monolithic half-bridge GaN power stage with elevated performance level shifting technique is proposed to operate reliably at high switching frequency. The challenges of the monolithic half-bridge topology will be discussed in detail in Section II. Section III presents the key circuit architectures and concepts. Implementation results and conclusions are given in Sections III and IV, respectively.

Fig. 1. Multi-phase switching power converter for envelope tracking and proposed monolithic GaN power stage.

II. Challenges in High Frequency Half-bridge Topology

As shown in Fig. 1, the proposed monolithic GaN power stage can be used for multi-phase high frequency envelope tracking applications, as well as similar DC-DC conversion. As the switching frequency and load current increase, the design of the half-bridge driver becomes more challenging.
A. Timing Match

In envelope tracking applications, the single phase switching frequency can reach 25MHz or higher, and the on-time $T_{ON}$ (pulse width) may be less than 10ns. With such a narrow on-time, the propagation delay mismatch between the rising and falling edges $T_{d_{\text{Mis}}}$ may significantly distort pulse, varying the expected duty ratio or even missing pulse. Moreover, the dead time $T_{\text{dead}}$ is typically much smaller than $T_{ON}$. Inaccurate sufficiently ON-OFF delay matching ($L_{\text{off}}$-$H_{\text{on}}$/$H_{\text{off}}$-$L_{\text{on}}$) between high and low side channels may result in shoot-through.

B. Common Mode Transient Noise

Consider the monolithic GaN level shifter [14] shown in Fig. 2 as an example. With the high speed switching of GaN HEMTs, the $dv/dt$ transient on switch node $V_{SW}$ causes an unexpected phase lag in the level shifter, which may distort the transmitted signal or induce a false trigger. Latches are commonly used in level shifters to guarantee communication reliability [15], having an intrinsic flaw to increase propagation delay. Considering the common trade-off between propagation delay and common mode transient immunity (CMTI), a level shifter with both low propagation delay and high CMTI capability is always preferred in high frequency applications.

C. Missing Pulse During Deadtime Operation

Fig. 3 depicts an easily overlooked risky scenario in the design of level shifters in the half-bridge topology. During the deadtime operation, low side power HEMT becomes reversely conductive, and the switching node $V_{SW}$ falls to a negative voltage. In such a case, the level shifter output voltage $V_{\text{drop}}$ cannot be lower than ground $GND$ or reach the threshold voltage $V_{\text{th}}$ of the receive circuit, resulting in missing pulse. If not addressed, the fault could lead to fatal results.

III. Circuit Implementations

A. Proposed Level Shifting Technique

Fig. 4 shows a schematic of the proposed level shifter, which consists of a receiver, a main pull-down and negative voltage pull-down circuit.

As shown in Fig.5(a), when $V_{PWM}$ changes from low to high, $V_{x,y}$ can be pulled to $GND/SW$ to turn off $Q_1$, and $R_{\text{Pull up}}$ determines the leakage current. Fig.5(b) shows the circuit operation in the $V_{PWM}$ low stage. In this period, $V_s$ is pulled by $R_{\text{Pull up}}$, and the rising of $V_y$ can be speeded up by buffer HEMT $Q_1$, which provides a stronger driving ability and lower propagation delay. Hence, under the same delay requirement, a larger $R_{\text{Pull up}}$ is allowed.

Considering the communication reliability, a higher CMTI capability can be achieved with a lower resistance of $R_{\text{Pull up}}$, but this also results in a larger leakage current. Therefore, the shielding capacitors $C_{\text{shield}}$ are designed and shown in Fig.5(c), which can couple the $dv/dt$ transient to $V_{x,y}$ and cancel the voltage drop caused by the parasitic capacitance $C_{pz}$ and $R_{\text{Pull up}}$. Similarly, a larger $R_{\text{Pull up}}$ can be adopted for the same CMTI requirement.

Given the above, the use of the proposed level shifter receiver with buffer HEMT $Q_1$ and shield capacitance $C_{\text{shield}}$ reduces the current consumption of the circuit without incurring additional propagation delay nor sacrificing its CMTI capability.

The operation of the negative voltage pull-down circuit and its timing diagram are shown in Fig. 6 and 7, respectively. When $V_{PWM}$ changes form low to high, the switching node $V_{SW}$ still stays at negative voltage(-3V),
and $V_{NV\,EN}$ is pulled up close to $GND$ by turning on $Q_{10}$ and $Q_{11}$. The voltage difference between $V_{NV\,EN}$ and $V_{SW}$ drives $Q_{8}$ and $Q_{9}$ to form pull-down current $I_{NV}$. It is important to note that $Q_{4}$ and $Q_{5}$ have to be turned off by $V_{MCTRL}$ to prevent the current competition between $I_{NV}$ and $I_{MAIN}$. During this interval, $V_{X,Y}$ can be pulled down to $V_{SW}$ to preserve the integrity of the PWM signal. After the high side power HEMT is switched on, $V_{SW}$ swiftly moves up to $V_{IN}$, and the main pull-down circuit is working again. $Q_{12}$ protects the gate-source voltage of $Q_{8}$ and $Q_{9}$ from excessive negative voltage when $V_{SW}$ is pulled up. $Q_{13}$ is designed to reset the $V_{NV\,EN}$ to $V_{SW}$ at the falling edge of $V_{SW}$.

**Fig. 6.** Operation of negative voltage pull-down circuit.

**Fig. 5.** Operation of the proposed level shifter. (a)$V_{PWM}$ changes from low to high. (b)$V_{PWM}$ changes from high to low. (c)Level shifter operation in high dv/dt transient.

**B. Monolithic Gate Driver**

In this work, the design idea of the driver is similar to prior work [11]–[14], hence the operation of the driver will be described only briefly.

Fig. 8 shows the structure of a widely adopted monolithic GaN inverter which can output a rail to rail inverse signal and a bootstrap signal. The schematic of monolithic gate driver is shown in Fig. 9, which provides strong driving capability by cascading inverters. An active GaN HEMT replaces the source resistor of last stage inverter to further increase the switching speed and reduce the power consumption. If the D-mode devices are provided in the GaN process, the power consumption can be significantly reduced by replacing the source resistor with a D-mode HEMT in series with a resistor.

**Fig. 7.** Timing diagram of negative voltage pull-down circuit when $V_{PWM}$ changes form low to high.

**Fig. 8.** Structure of the favored monolithic GaN inverter.

**Fig. 9.** Schematic of the monolithic GaN driver.

**IV. Implementation Results**

The proposed Monolithic GaN Power Stage is implemented in 0.25$\mu$m 15-V enhanced mode GaN (eGaN) process with an active area of 1250$\mu$m × 1600$\mu$m, as shown in Fig. 10.

Fig. 11 shows the simulated operating waveforms of the high and low side propagation (HIN to HOUT, LIN to LOUT) under different corners and temperatures. The simulation results show that the propagation delay of high and low side is between 1.9ns and 4.0ns, which means that the proposed power stage has extremely low propagation delay and can respond quickly to the controller.
The high side propagation delay simulations with different $V_{SW}$ are performed considering the variation of $V_{SW}$ affects the operating conditions of the level shifter. The simulated data is shown in Fig. 12 in a form of three graphs (the GaN simulation model has poor convergence, thus some data is missing). Under different simulation conditions, the high side propagation delay is within 6 ns, and the mismatch between the rising and falling edges does not exceed 2 ns, indicating that the proposed design can effectively avoid the pulse width distortion.

Table I sums up the simulated electrical characteristics (covering additional simulation conditions). It shows a propagation delay of no more than 6.5 ns, a delay mismatch below 2.5 ns, a pulse width distortion within 2 ns, a turn-on rise time $t_r$, and a turn-off fall time $t_f$ around 1 ns. In addition, the proposed design features 150 V/ns CMTI capability. These data demonstrate that the proposed power stage can effectively address the timing match and communication reliability challenges mentioned in Section II.

V. Conclusion

In this paper, we propose a monolithic GaN power stage with a novel level shifting technique that can achieve high communication reliability. Moreover, the propagation delays are carefully optimized to prevent shoot through and pulse width distortion. This means that system applications can mitigate the limitations of ultra-narrow pulse width and dead time. In conclusion, the proposed monolithic GaN power stage is a promising candidate in an industry trend toward higher power density and higher switching frequency.

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References


