A VCO-Based 2\textsuperscript{nd}-Order Continuous Time Sigma-Delta Modulator for Current-Sensing Systems

Yi-Ting Hsieh, Shih-Shuo Chang, Hao-Yun Lee, Ju-Yi Chen, and Shuenn-Yuh Lee

Department of Electrical Engineering
National Cheng-Kung University, Tainan, Taiwan
Outline

● Introduction
  • Motivation

● Circuit Design
  • VCO-based SDM
  • Close-loop Architecture of SDM
  • Proposed CTSDM Architecture
  • Nonlinearity Analysis
  • Circuit Implementation

● Measurement Result

● Comparison

● Conclusion
Outline

● **Introduction**
  • Motivation

● **Circuit Design**
  • VCO-based SDM
  • Close-loop Architecture of SDM
  • Proposed CTSDM Architecture
  • Nonlinearity Analysis
  • Circuit Implementation

● **Measurement Result**

● **Comparison**

● **Conclusion**
Introduction

● Sensor requirement
  • Wearable device
  • Edge computing
    - Current readout circuit
  • Electrochemistry application
Motivation

- Conventional Current Readout Circuit [1]
  - Trans-impedance amplifier
    - Straightforward circuit implementation

- Proposed concept of VCO-based 2\textsuperscript{nd}-order CTSDM
  - Direct current sensing [2]
Outline

- **Introduction**
  - Motivation

- **Circuit Design**
  - VCO-based SDM
  - Close-loop Architecture of SDM
  - Proposed CTSDM Architecture
  - Nonlinearity Analysis
  - Circuit Implementation

- **Measurement Result**

- **Comparison**

- **Conclusion**
VCO-based SDM

- Ring oscillator structure
  - Inverter chain
  - Intrinsic 1\textsuperscript{st} order noise-shaping
- Non-linearity of voltage to frequency coefficient ($K_v$)
  - Closed-loop system

![Diagram of 15-stage Ring CCO]
Closed-loop VCO-based SDM

- Reduce VCO input swing
- Multi-bit quantization ($D_{out}$)
  - Thermometer term
    - Mismatch of feedback DAC
- Dynamic element matching (DEM) technique is required

\[ V_{in}(t) \rightarrow + \rightarrow VCO \rightarrow \text{Quantizer} \rightarrow D_{out} \]

error signal
Dynamic Element Matching [3]

- Frequency domain
  - Data weighted averaging (DWA)
    - Loss of the integration capability

- Phase domain
  - Clocked averaging (CLA)
    - Dual VCO structure
CIFB Technique[4]

- **Current-sensing 2nd order VCO-based CTSDM**
  - 2nd order noising shaping
    - Current integrator + VCO-based phase integrator

- **CIFB architecture**

![Diagram of CIFB Technique]
Circuit Implementation

- Passive integrator + Dual-CCO structure

![Circuit Diagram]

- Current-steering DAC
- 15-stage Ring CCO
- Degeneration RDAC
- Thermometer-to-Binary Adder
- Decoder
- 4-bit DOUT
Degeneration RDAC [5]

- Digital feedback with variable $R^+$, $R^-$ to control branch current
  - Excess settling time
  - Losing CLA capability
Proportional Integral Technique [6]

- Simple circuit complexity
  - One feedback path
- Straightforward implementation

\[ I_{in} \rightarrow a_1 \rightarrow \frac{1}{s} \rightarrow a_2 \rightarrow \frac{1}{s} \rightarrow D_{out} \]

Proportional feedforward path

Integral path

\[ V_{in} \rightarrow G_m \rightarrow V_{out} \]

\[ a_1 + a_2 + a_3 \]
Closed-loop System Architecture

- Cascade of integrators with distributed feedback (CIFB)
  \[
  NTF(s) = \frac{1}{1 + a_2'H(s) + a_1'a_2'H(s)^2}
  \]

- Proportional-integral (PI) feedforward
  \[
  NTF(s) = \frac{1}{1 + a_2a_3H(s) + a_1a_2H(s)^2}
  \]

Same noise shaping ability

\[
a_1' = \frac{a_3}{a_1}, a_2' = a_2a_3
\]
This Work

- **Current-sensing 2\textsuperscript{nd} order VCO-based CTSDM**
  - 2\textsuperscript{nd} order noising shaping
    - Proportional-integral (PI) integrator + VCO-based phase integrator
    - Only one feedback path

![Diagram of current-sensing 2\textsuperscript{nd} order VCO-based CTSDM](image)
System Synthesis

- Matlab SDM toolbox

<table>
<thead>
<tr>
<th>2\textsuperscript{rd}-oder CTSDM</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>OSR</td>
<td>64</td>
</tr>
<tr>
<td>Quantization Level (nelv)</td>
<td>16 (4-bit)</td>
</tr>
<tr>
<td>Out-of-band Gain (OBG)</td>
<td>2.5</td>
</tr>
<tr>
<td>Order</td>
<td>2</td>
</tr>
<tr>
<td>$a_1$</td>
<td>0.11285</td>
</tr>
<tr>
<td>$a_2$</td>
<td>5.8907</td>
</tr>
<tr>
<td>$a_3$</td>
<td>0.2037</td>
</tr>
</tbody>
</table>
Proposed CTSDM Architecture

- **PI current integrator**
  - Charging $R_s$ and $C_{in}$ path with residue current ($I_{in} - I_f$)

- **Dual-CCO phase integrator**
  - CLA technique
Nonlinearity Analysis

- Input swing of $G_m$-CCO
  - Keep voltage to frequency coefficient ($K_v$) linear
Nonlinearity Analysis

- Harmonic Distortion
  - Input signal \( x(t) = A \cos(\omega t) \)
  - Output signal \( y(t) = \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) \)

\[
\frac{\alpha_2 A^2}{2} \ast \alpha_1 @ \ast \frac{3\alpha_3 A^3}{4} (\text{bnr} \Delta s \ast \frac{\alpha_2 A^2}{2} \text{bnr}'1 \Delta s \ast \frac{\alpha_3 A^3}{4} \text{bnr}'2 \Delta s)
\]

\[
THD = \left( \frac{\alpha_2 A^2}{2} \right)^2 + \left( \frac{\alpha_3 A^3}{4} \right)^2
\]

\[
\text{HD2} \quad \text{HD3}
\]
Nonlinearity Analysis

- Nonlinearity topology in Matlab

\[ \frac{\alpha_2}{\alpha_1} = \frac{-HD^2}{10 \, 20} \left( \frac{\alpha_3}{\alpha_1} \right) A \]

\[ \frac{\alpha_3}{\alpha_1} = \frac{-HD^3}{10 \, 20} \]

\[ \frac{-HD^3}{20} \cdot 0.25A^2 - 0.75A^2 \cdot 10 \]

If \( I_{in} \) + \( a_1 * f_s \)

\( a_3 \)

IDAC
Linearity Verification

- Simulated output spectrum of the nonlinearity model with different HD2 / HD3
Nonlinearity Analysis

- DC sweep $V_c$ (VCO input signal)
  - Use "polyfit" by Matlab to fit the curve
  - $K_v = 1.2$ MHz/V , $HD2 = -60.17$ dB , $HD3 = -61.35$ dB
Proposed CTSDM Topology

- **PI current integrator**
  \[ H_1(s) = a_3 + \frac{a_1 f_s}{s} \]

- **Dual-VCO phase integrator**
  \[ H_2(s) = \frac{\Delta \varphi(s)}{\Delta V_{in}} = \frac{a_2 f_s}{s} \]
Proposed CTSDM Architecture

- **PI current integrator**
  - \( \frac{\Delta V_c}{I_{in}} = R_s + \frac{1}{sC_{in}} \)
  - \( \frac{\Delta V_c}{V_{in}} = G_{m1}R_s + \frac{G_{m1}}{sC_{in}} = H_1(s) = a_3 + \frac{a_1 f_s}{s} \)

- **Dual-CCO phase integrator**
  - \( \frac{\Delta \varphi(s)}{\Delta V_{Gm-cco}} = \frac{2\pi K_v}{s} = H_2(s) = \frac{\Delta \varphi(s)}{\Delta V_{in}} = \frac{a_2 f_s}{s} \)

![Diagram of the Proposed CTSDM Architecture](image)
Coefficients Realization

- Compared with the proposed architecture (Assumed $I_{in} = 2 \mu A$)
  
  \[
  \frac{V_{in}}{V_{Gm-CCO}} = \frac{V_{Am}}{V_{Am-CCO}} \quad ; \quad G_{m1} = \frac{I_{in}}{V_{in}} = \frac{I_{in}}{V_{Gm-CCO} \cdot V_{Am}} = 3.63 \, \mu S \quad (1)
  \]

  \[
  C_{in} = \frac{G_{m1}}{a_1 f_s} = 25.12 \, pF \quad (2)
  \]

  \[
  R_s = \frac{a_3}{G_{m1}} = 56.13 \, k\Omega \quad (3)
  \]
Circuit Implementation

- PI integrator + Dual-VCO structure
- Complementary current-steering DAC
<table>
<thead>
<tr>
<th>Specification</th>
<th>This work</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage (V)</td>
<td>1.2</td>
</tr>
<tr>
<td>$I_{in}$ (µA)</td>
<td>± 2</td>
</tr>
<tr>
<td>Input Frequency (Hz)</td>
<td>2421.875</td>
</tr>
<tr>
<td>Sampling Frequency (MHz)</td>
<td>1.28</td>
</tr>
<tr>
<td>Bandwidth (kHz)</td>
<td>10</td>
</tr>
<tr>
<td>SNDR (dB)</td>
<td>81.36</td>
</tr>
<tr>
<td>Power Consumption (µW)</td>
<td>13.2</td>
</tr>
</tbody>
</table>

* Without noise simulation
Noise Analysis

- `.tran noise`
- `SNDR = 79.43 dB`
Outline

● Introduction
  • Motivation

● Circuit Design
  • VCO-based SDM
  • Close-loop Architecture of SDM
  • Proposed CTSDM Architecture
  • Nonlinearity Analysis
  • Circuit Implementation

● Measurement Result

● Comparison

● Conclusion
Chip Layout And Microphotograph

● 180nm CMOS 1P6M process
  • Core area occupied 0.21mm²
Measurement

● Environment Setup

Waveform Generator (Keysight 33500B)

Audio Analyzers (Audio Precision APX525)

Battery

Regulator

CTSDM

EUT

Logic Analyzer (Agilent 16962A/16911A)
Measurement Result

- $I_{in} = \pm 2 \, \mu A$, $R_s = 56.13 \, k\Omega$, $C_{in} = 25.12 \, pF$

<table>
<thead>
<tr>
<th>Specification</th>
<th>This work</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage (V)</td>
<td>1.2</td>
</tr>
<tr>
<td>$I_{in} , (\mu A)$</td>
<td>$\pm 2$</td>
</tr>
<tr>
<td>Input Frequency (Hz)</td>
<td>2421.875</td>
</tr>
<tr>
<td>Sampling Frequency (MHz)</td>
<td>1.28</td>
</tr>
<tr>
<td>Bandwidth (kHz)</td>
<td>10</td>
</tr>
<tr>
<td>SNDR (dB)</td>
<td>63.7</td>
</tr>
<tr>
<td>Power Consumption (µW)</td>
<td>14.6</td>
</tr>
</tbody>
</table>

![Power Spectrum Diagram](image-url)
Measurement Result

- $I_{in} = \pm 12.5 \, \mu A$, $R_s = 11.23 \, k\Omega$, $C_{in} = 125.6 \, pF$

<table>
<thead>
<tr>
<th>Specification</th>
<th>This work</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage (V)</td>
<td>1.2</td>
</tr>
<tr>
<td>$I_{in}$ (µA)</td>
<td>$\pm 12.5$</td>
</tr>
<tr>
<td>Input Frequency (Hz)</td>
<td>2421.875</td>
</tr>
<tr>
<td>Sampling Frequency (MHz)</td>
<td>1.28</td>
</tr>
<tr>
<td>Bandwidth (kHz)</td>
<td>10</td>
</tr>
<tr>
<td>SNDR (dB)</td>
<td>74.6</td>
</tr>
<tr>
<td>Power Consumption (µW)</td>
<td>44.8</td>
</tr>
</tbody>
</table>

![Power Spectrum Diagram]

- $F_{in} = 2421.875 \, Hz$
- $I_{in} = \pm 12.5 \, \mu A$
- SNDR = 74.6 dB
- $BW = 10 \, kHz$
- SFDR = 81.54 dB
Dynamic Range

- DR = 77.27 dB

Input = Sinusoidal @ 2.421 kHz
Peak SNDR = 74.6 dB
Outline

● Introduction
  • Motivation

● Circuit Design
  • VCO-based SDM
  • Close-loop Architecture of SDM
  • Proposed CTSDM Architecture
  • Nonlinearity Analysis
  • Circuit Implementation

● Measurement Result

● Comparison

● Conclusion
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Tech. (nm)</td>
<td>180</td>
<td>180</td>
<td>180</td>
<td>350</td>
<td>180</td>
<td>180</td>
</tr>
<tr>
<td>Supply (V)</td>
<td>1.2</td>
<td>1.8</td>
<td>5 / 1.8</td>
<td>1.5</td>
<td>1.2</td>
<td>1.8</td>
</tr>
<tr>
<td>F&lt;sub&gt;S&lt;/sub&gt; (Hz)</td>
<td>1.28 M</td>
<td>25.6 k</td>
<td>160 k</td>
<td>500 k</td>
<td>-</td>
<td>25.6 k</td>
</tr>
<tr>
<td>OSR</td>
<td>64</td>
<td>64</td>
<td>64000</td>
<td>2048</td>
<td>-</td>
<td>64</td>
</tr>
<tr>
<td>BW (Hz)</td>
<td>10 k</td>
<td>200</td>
<td>1.25</td>
<td>122</td>
<td>around DC</td>
<td>200</td>
</tr>
<tr>
<td>Input Range</td>
<td>± 3 µA</td>
<td>± 15 µA</td>
<td>± 15 µA</td>
<td>4 µA</td>
<td>0.2 µA~3 µA</td>
<td>± 5 µA</td>
</tr>
<tr>
<td>SNDR (dB)</td>
<td>63.7</td>
<td>74.6</td>
<td>67</td>
<td>-</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>DR (dB)</td>
<td>-</td>
<td>77.27</td>
<td>73</td>
<td>73</td>
<td>88.9</td>
<td>108</td>
</tr>
<tr>
<td>Power (µW)</td>
<td>14.6</td>
<td>44.8</td>
<td>60</td>
<td>340</td>
<td>16.8</td>
<td>16</td>
</tr>
<tr>
<td>Power Eff. 1</td>
<td>0.49</td>
<td>0.8</td>
<td>0.9</td>
<td>0.06</td>
<td>0.26</td>
<td>0.75</td>
</tr>
<tr>
<td>FOM&lt;sub&gt;w&lt;/sub&gt; 2 (J/conv.)</td>
<td>0.448p</td>
<td>0.375 p</td>
<td>41.09 p</td>
<td>37.25n</td>
<td>3.02p</td>
<td>38.95p</td>
</tr>
<tr>
<td>FOM&lt;sub&gt;s&lt;/sub&gt; 3 (dB)</td>
<td>154.36</td>
<td>160.76</td>
<td>138.23</td>
<td>108.65</td>
<td>157.51</td>
<td>155.96</td>
</tr>
</tbody>
</table>

2 FoM<sub>w,DR</sub> = Power / 2*BW*2<sup>(DR-1.76)/6.02</sup>
3 FoM<sub>s,DR</sub> = DR + 10log (BW / Power)
Outline

- **Introduction**
  - Motivation

- **Circuit Design**
  - VCO-based SDM
  - Close-loop Architecture of SDM
  - Proposed CTSDM Architecture
  - Nonlinearity Analysis
  - Circuit Implementation

- **Measurement Result**

- **Comparison**

- **Conclusion**
Conclusion

- Direct current sensing readout circuit
- Amplifier-less structure which is highly reconfigurable for different system specifications
- PI architecture is adopted to significantly reduce the circuit complexity
- FoMs 160.76 dB and high power efficiency 0.8 with a relatively low oversampling ratio of 64


Thanks for your listening