An ISFET Array for Ion Multiplexing with an Integrated Sensor Learning Algorithm

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Abstract—Widening the range of targets for ion-sensitive field-effect transistors (ISFETS) fabricated in unmodified CMOS technology has been enabled by the deposition of polymeric ionophore membranes at the surface, requiring specific sensor training. We present a novel ISFET array with on-chip multiplexing capabilities to perform offline training and real-time sensing on a single substrate, enabling analogue averaging for low noise sensing and reducing post-processing. The analogue front-end pixels rely on a modular current-mode spatial averaging (CMSA) circuit, producing an averaged sensor output per cluster based on a switching matrix integrated within the array. At the output stage, a weak inversion active resistor implements an ELIN system to guarantee linearity, reaching an expected sensitivity of 160 mV/pH with a gain of 3, when designed using a 0.18 µm standard CMOS technology. Based on calibration data for the ion targets, an on-chip training algorithm determines the sensitivity of each pixel to each ion, identifies sensing regions corresponding to polymeric membranes at the surface and sets the pixel connectivity through the switching matrix.

I. INTRODUCTION

Chemical sensors fabricated in Complementary Metal-Oxide-Semiconductor (CMOS) technology have presented key benefits for integration, low cost, scalability and robustness [1]. In particular, the Ion-Sensitive Field-Effect Transistor (ISFET) relies on the structure of the MOSFET which allows for the design of analogue front-end topologies with on-chip signal processing while keeping small dimensions. When implementing the ISFET in unmodified CMOS technology [2], the surface passivation layer is usually made of Si$_3$N$_4$ which inherently provide pH sensitivity to the ISFET. This has justified the drive of ISFET array chips towards DNA sequencing [3] or detection [4].

We have recently demonstrated the possibility of widening the range of sensing of the ISFET to multiple ions on the same substrate by combining large ISFET arrays integrating more than 1,000 sensors with polymeric ionophore membranes to grant sensitivity to other ions such as potassium, sodium and calcium [5]. The novelty of this approach lies within (1) the versatility of sensing, allowing for more membranes or more pixel coverage depending on the application and performing sensor averaging within each sensing region, and (2) the possibility of integrating thousands of sensors in a microfluidic setting to monitor ion concentrations in real-time. Indeed electrochemical sensing matches requirements for portability of healthcare devices, where several works involving optical sensing have failed due to the requirement for bulky instrumentation for light source or detection. This was the case for Sato et al. [6], reporting optical sensing of multiple ions inside a microchannel, and Lapresta-Fernandez et al. [7], focusing on one-shot optical sensors for potassium and magnesium. On the other hand, previous publications relying on electrochemical sensing have been limited to only a few sensors [8], [9].

In this new setup, pixels within the same array carry sensitivity to all target species, defined by surface functionalisation, and must be calibrated through an off-line process. There is an opportunity to implement specific algorithms to train the sensor array towards real-time monitoring of ion concentration through an off-line calibration. In this work, we refer to this process as sensor learning. Although this calibration can be performed externally using a microcontroller or field-programmable gate array (FPGA), integrating sensing and learning on the same substrate allows for (1) improved resolution through averaging at the level of the analogue front-end and (2) relaxed bandwidth requirements through on-chip data compression. This represents the first step towards on-chip sensor learning in the context of a large ISFET array for multi-ion imaging.

In this paper, we report the first architecture of large-scale ISFET array with integrated clustering scheme for multi-ion sensing. The system was developed as an analogue front-end ISFET array with switching matrix and a synthesised digital back-end as spatial calibration algorithm. In Sec. II, we provide a brief introduction of the ISFET. Secs. III and IV focus on the analogue architecture, respectively at a pixel and array level. The training algorithm is described in Sec. V and Sec. VI briefly discusses the full system and the performance.
II. THE ISFET FOR MULTI-Ion SENSING

The ISFET is a solid-state sensor where the gate is tied to a reference electrode in contact with a solution and the oxide is replaced with an insulating layer. The layer captures ions to balance charge concentration in the channel, causing a variation in the threshold voltage of the device. A solution containing several ions of varying concentrations cannot be considered ideal, hence the model of the ISFET must be established based on the activity $a_i$ of each ion $i$ [11]. The chemical contribution in the threshold voltage is then expressed as

$$V_{chem} = \Gamma - \alpha S_N \log(x_i) = \Gamma' - \alpha S_N \log(a_i)$$

where the activity is related to the concentration through the activity coefficient $\gamma_i$ following $a_i = \gamma_i x_i$, $\Gamma = \Gamma' - \alpha S_N \log(\gamma_i)$ groups all non ionic related terms$^1$ and $\alpha$ reflects the deviation from the Nernstian sensitivity $S_N = (2.3RT)/F \approx 59 \text{ mV}$ at ambient temperature.

For low power operation, the ISFET is biased in weak inversion, hence when $V_{ds} < 4U_i$, the current is expressed as an exponential dependence of the floating gate.

$$I = I_0 \exp \left( \frac{V_{g's} - x_i}{nU_i} \right)$$

Sensor non-idealities should be mentioned for the sake of completeness, particularly sensor offset originating from trapped charge which requires calibration to initialise the array at a baseline frame [1].

III. MODULAR PIXEL ARCHITECTURE FOR CURRENT AVERAGING

A. Pixel topology with voltage-clamped front-end

The pixel implementation is based on a voltage-clamped readout structure [12] shown in Fig. 6(a). In this configuration the drain voltage of the ISFET $Q_0$ through high gain single stage amplifier formed by $Q_1$. As a result, any potential change in the solution generates a change in the current flowing through the ISFET. Compared to [12], transistors $Q_0, Q_1$ and $Q_2$ were made reduced to 2 $\mu$m / 2 $\mu$m to match scaling requirements, produce a small pixel and drive all transistors in weak inversion operation. A network of current mirrors $Q(4:7)$ provide the bias current for the front-end at 1 nA. The chemically dependent output current also feeds a switch-controlled current mirror.

Each pixel integrates two switches to enable connectivity with its neighbour and sum current contributions from pixels in the same cluster. The switches $Q(8,9)$ and respectively connected to the south and east pixels. By extension, the north and west pixels contain the switch for connectivity with the current pixel. This solution allows the pixel connectivity to be fully controlled by the sensor learning algorithm through a switching matrix, enabling a versatile ISFET array where pixels can be connected to form clusters. The summed current within each cluster is then mirrored to an output stage through a third switch $Q10$.

B. Compensation Schemes

To compensate for sensor offset, the pixel uses a similar scheme to the one proposed in [10], whereby the source voltage is controlled through a DAC to calibrate the gate-source voltage $V_{g's}$ of the ISFET. This technique was motivated by recent work [13] demonstrating spatial correlation in sensor offset associated with trapped charge throughout the array, and hence supports the hypothesis that offsets values within a cluster of sensor exhibit low deviation.

IV. ARRAY-LEVEL CMSA CIRCUIT BASED ON COMPANDING

A. Spatial averaging

The concept for array-level spatial averaging is illustrated in Fig. 2(b) for a small structure of 9 pixels. Pixels of the same cluster are connected through the switches and the

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$^1$ $\Gamma$ is equivalent to $\gamma$ in our previous publications but has been redefined for clarity.
gate voltage biases the output current mirror, replicating the average current. The output decoder (row decoder/column decoder) was implemented to select an output current of one pixel or an averaged current of several pixels in a cluster.

The configuration uses the concept of companding by compressing the chemical voltage exponentially through the in-pixel ISFET operated in weak inversion and expanding logarithmically at the output stage when converting the averaged current to an output voltage through the active resistors. The architecture can hence be qualified as a non-linear (ELIN) system. The input-output relationship can be derived as follows. The output current of each pixel is given by

$$I_{out} = I_o \exp \left( \frac{V_{g's}}{nU_T} \right) \propto \exp \left( \frac{V_{pH}}{nU_T} \right)$$

The output stage is a current mirror with a weighted value of the average current. The circuit produces a voltage determined by the active load which are series diode-connected transistors operated in weak inversion. As a result, the output voltage for each cluster is given by

$$V_{out} = \log \left( \frac{1}{N} \sum_{i=1}^{N} I_{out} \right)$$

### B. Simulated results

The analogue front-end pixel architecture and the array peripherals are simulated for a TSMC 0.18 µm process in Cadence Virtuoso. Figs. 3(a) and 3(b) highlight the pH sensitivity of the ISFET and the exponential dependence originating from the weak inversion operation. In the range of interest and assuming an ISFET intrinsic pH sensitivity of 30 mV/pH, the pH-current sensitivity of the pixel is 5.27 dB/pH.

Fig. 3(c) demonstrates the operation of the active load operated in weak inversion, highlighting a logarithmic dependence between the current and the voltage, and the voltage output for each cluster is given by

### V. SENSOR LEARNING ALGORITHM

The chip integrates an offline sensor learning clustering algorithm to identify selectivity and sensitivity of all sensors to each ion and set the array connectivity. Offline training is performed by flowing solutions with a decade change in the concentration of each target ion and processing the calibration data. The digital core integrates both the algorithm and a memory array to store the calibration value generated by the sensor training algorithm. The requirements for 3-dimensional clustering drove the choice of algorithm to Density-Based Spatial Clustering of Applications with Noise (DBSCAN) [14].

The training workflow is illustrated in Fig. 4. The algorithm starts with a pixel located at the corner of the array, which is optimal in the likely case that it is covered by a membrane. If the pixel has not been visited, its neighbours are identified by quantifying the distance with each neighbour in terms of X coordinates, Y coordinates, and voltage output. Key parameters for the cluster identification include the threshold $\varepsilon$ for the distance between a pixel and its neighbour for inclusion as part of the same cluster and the minimum number of pixels $N_{min}$ in a region to be considered a cluster. This iteration is then repeated for the next pixel which has not been classified and ends once the last pixel is reached.

Previous work on ISFET front-end pixel architectures [10] has integrated memory inside each pixel for sensor compensation. Building up from this approach, we store the outcome of the training in each pixel in a 12-bit SRAM. The integration of the digital memory with the analogue sensing front-end brings the opportunity of scalability to lower process nodes as well as increased sensing area to boost the sensing signal [1]. 9 bits are dedicated to storing the pixel output for the initial calibration and 3 more bits are used during the algorithm to flag visited pixel, neighbour pixel, and temporary neighbor

![DBSCAN state diagram](image-url)
pixel. The algorithm is written in VHDL for on-chip synthesis. As a proof-of-concept, we provide sensing data from a previously fabricated array [15] with ionophore membranes to grant sensitivity to potassium ($K^+$), sodium ($Na^+$) and calcium ($Ca^{2+}$). Fig. 5 bottom shows the spatial output of the array for each ion run. We apply the DBSCAN algorithm on MatLab and obtain the mapping of Fig 5 top, where the yellow area determines the location of the target membrane. The remaining area is considered non-covered and hence pH sensitive. The algorithm also stores training data containing the sensitivity of each pixel to each ion. For the case of integrated algorithm, these areas will define the switching connectivity of the pixels.

VI. SYSTEM ARCHITECTURE AND PERFORMANCE

Fig. 2(b) includes the peripheral components of the system, including DAC for the offset compensation through the ISFET source voltage, the synthesised training core and the serial peripheral interface (SPI). The layout of the pixel and the system are shown in Fig. 6.

Specifications of the sensing system are listed in Table I. The table highlights the small pixel size with memory and sensor front-end, a low power consumption and

VII. CONCLUSION

We presented a modular ISFET array with offline sensor learning algorithms for multi-ion detection. A CMSA circuit performs spatial averaging between pixels of the same cluster for white noise reduction, and the system provides compensation for sensor offset through a global source voltage compensation mechanism. Each cluster implements an ELIN system to provide a single sensor output per cluster. Training is achieved by implementing a DBSCAN clustering algorithm on-chip, which was demonstrated with experimental results. Overall, this work is the first step towards multi-ion sensor training integrated on a single substrate, reducing the requirements for post-processing and enabling real-time measurements.
REFERENCES


