IEEE ISAF 2023
IEEE International Symposium on Applications of Ferroelectrics (ISAF)
International Symposium on Integrated Functionalities (ISIF)
& Piezoresponse Force Microscopy Workshop (PFM)

Enhanced functionality of semiconductor devices enabled by ferroelectricity in hafnium oxide

Thomas Mikolajick

NaMLab gGmbH, Dresden, Germany, thomas.mikolajick@namlab.com

IHM, TU Dresden, Dresden, Germany, thomas.mikolajick@tu-dresden.de

Outline

Introduction

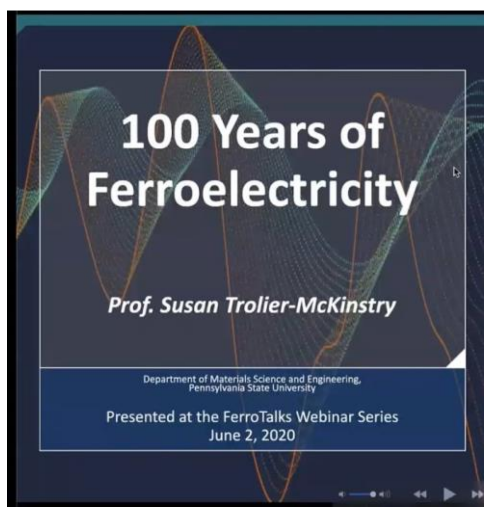
- Ferroelectric Materials for Semiconductor Devices
- Basic Ferroelectric Memory Devices
- Ferroelectric enhanced Devices for Beyond von-Neumann Computing
- Ferroelectric Devices for other Applications
- Summary and Conclusion

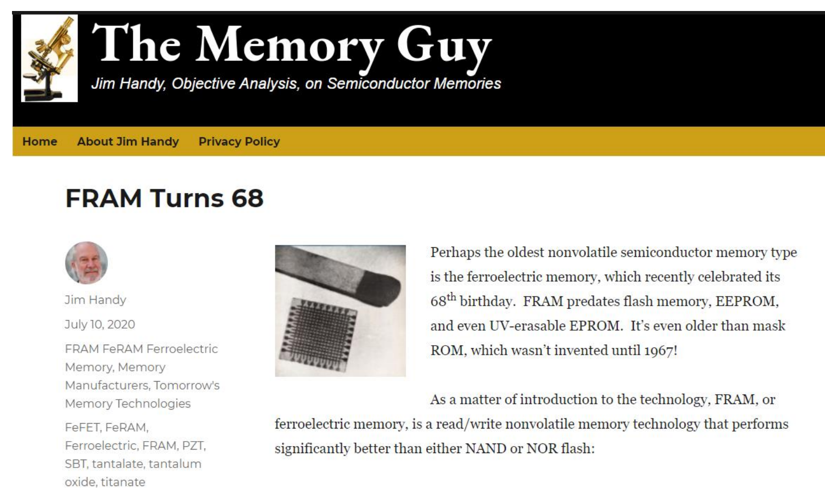
Introduction – History of ferroelectric memories

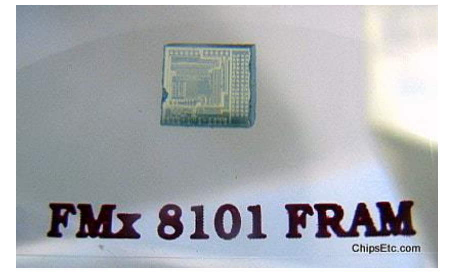
103 years of ferroelectricity

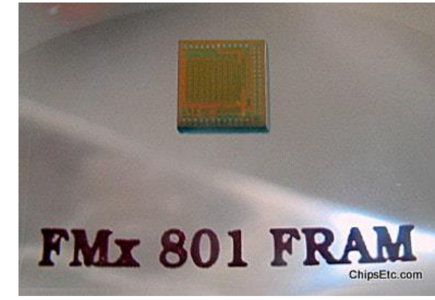
71 years of ferroelectric memory

30 years of commercial FRAM









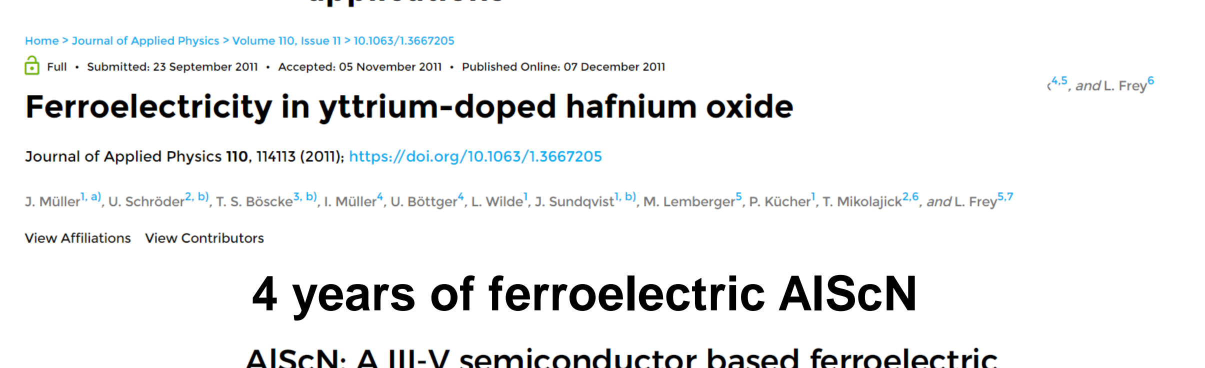
1993

Introduction of first commercially available FRAM product 512x8 by Ramtron (now Infineon)

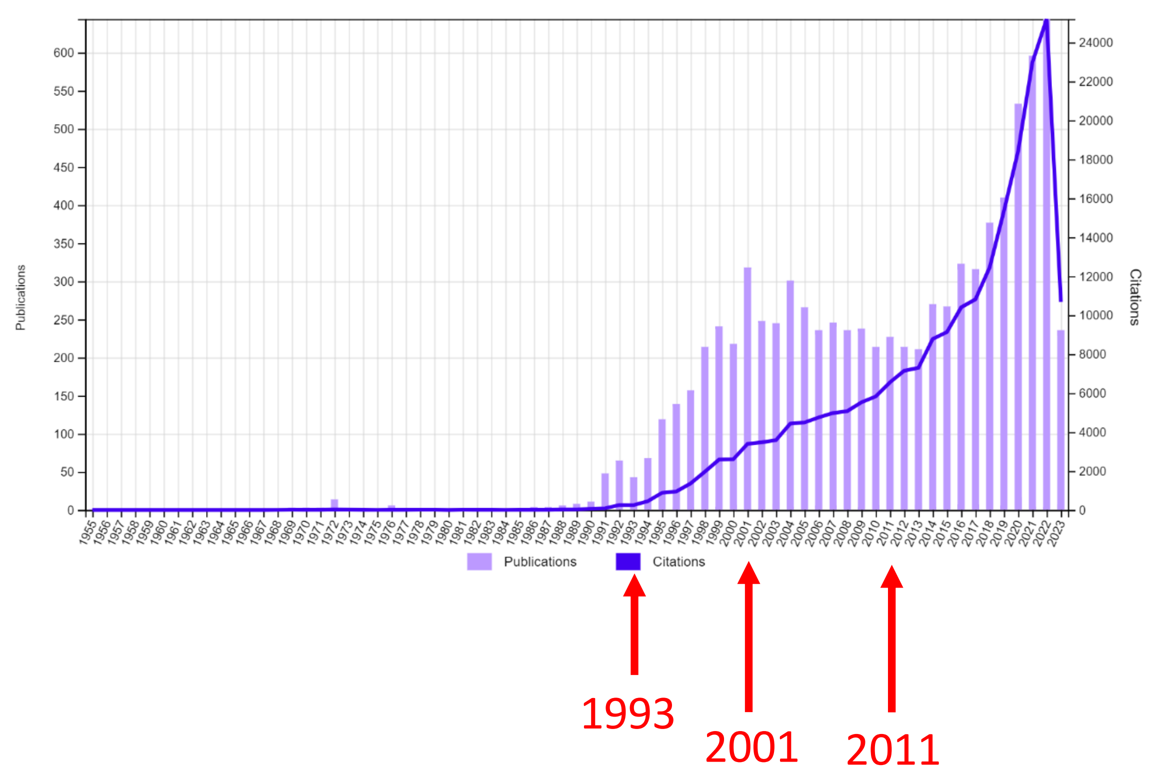
- Ferroelectricity in Rochelle salt has been discovered 103 years ago by Josef Valasek
- Ferroelectric memories have been invented 71 years by Dudley Allen Buck
- FRAM is commercially available since 30 years. First products were offered by Ramtron

Introduction – First report of ferroelectric hafnium oxide

12 years of ferroelectric hafnia



Publications and citations on the topic "ferroelectric memories"



4 years of ferroelectric AlScN

AlScN: A III-V semiconductor based ferroelectric

Cite as: J. Appl. Phys. 125, 114103 (2019); doi: 10.1063/1.5084945
Submitted: 7 December 2018 · Accepted: 28 February 2019 ·
Published Online: 18 March 2019

Simon Fichtner,[1,2] Niklas Wolff,[3] Fabian Lofink,[2] Lorenz Kienle,[3] and Bernhard Wagner[1,2]

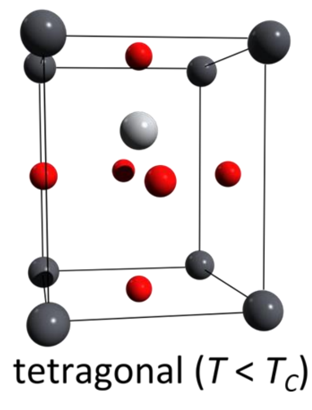
- Ferroelectric hafnium oxide was reported 12 years ago
- Research activities have reached new heights by having a CMOS compatible ferroelectric at hands
- Ferroelectric AlScN was reported only 4 years ago

Outline

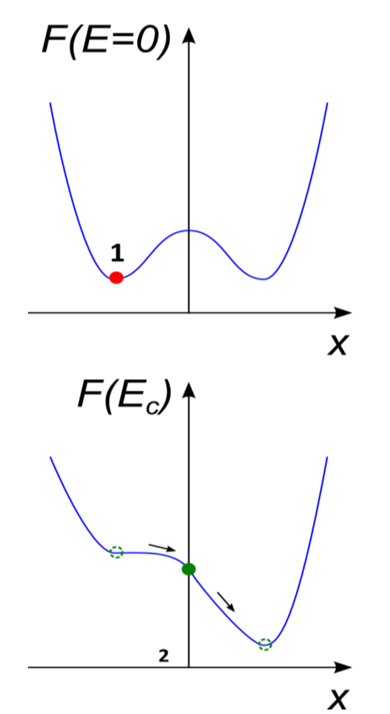
- Introduction
- Ferroelectric Materials for Semiconductor Devices
- Basic Ferroelectric Nonvolatile Memory Devices
- Ferroelectric enhanced Devices for Beyond von-Neumann Computing
- Ferroelectric Devices for other Applications
- Summary and Conclusion

Ferroelectrics – Reminder

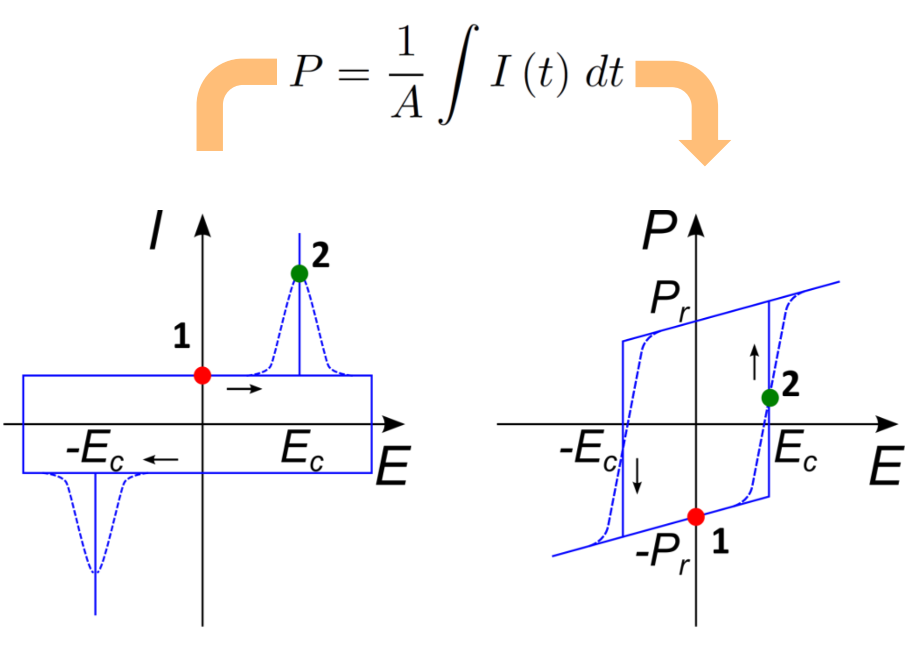
Ferroelectric crystal



Double well potential of ferroelectric material

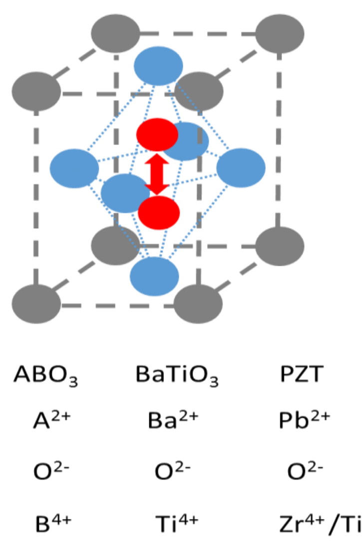
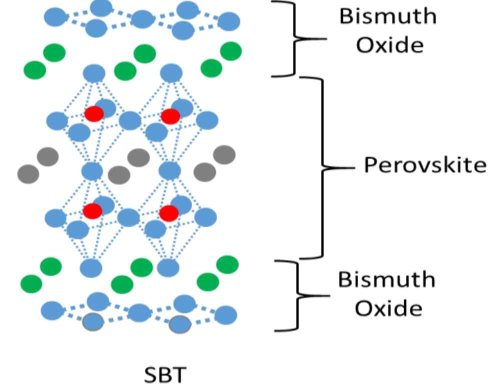
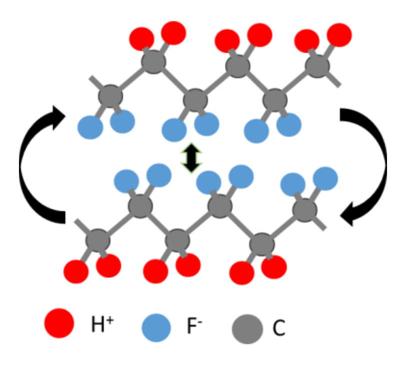
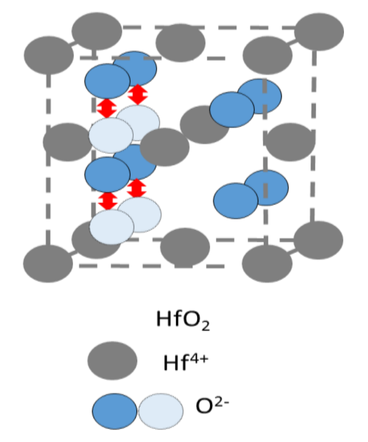
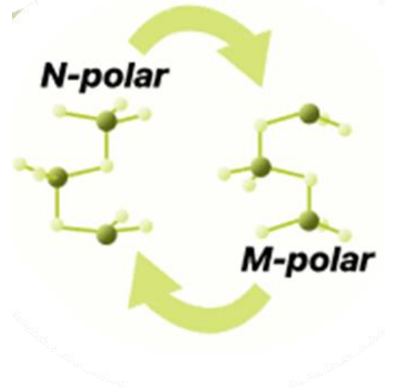


Hysteresis



- Ferroelectrics have two stable polarization states that can be switched by applying an electric field → no inefficiency during writing → lowest write energy of known nonvolatile concepts

Ferroelectrics – Materials for Semiconductor Devices

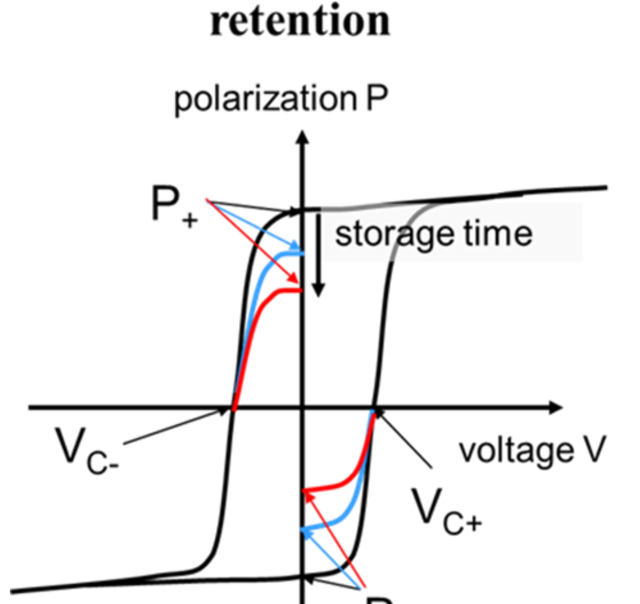
	Lead-Zirconium Titanate (PZT)	Strontium-Bismuth-Tantalate (SBT)	Polyvinylidenflouride (PVDF)	Orthorhombic Hafnium Oxide ($X:HfO_2$)	Aluminum Scandium Nitride (AlScN)
					

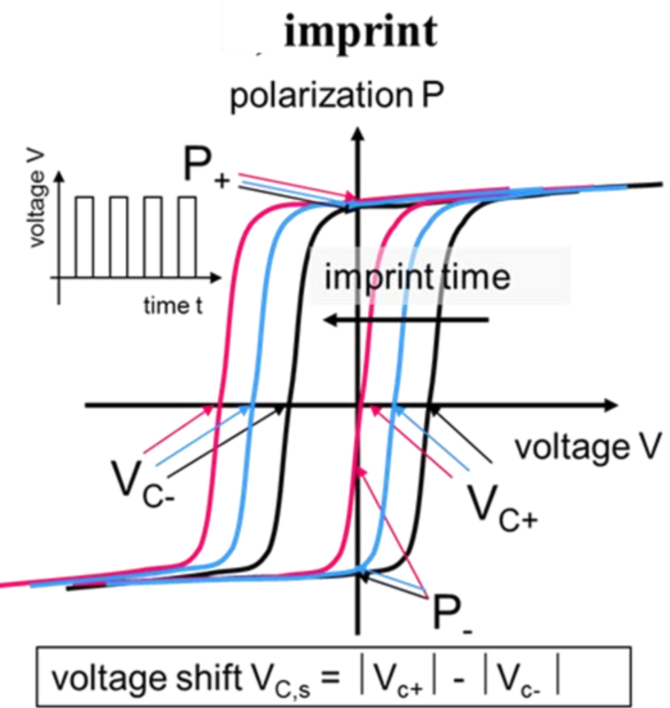
U. Schröder et al., Nature Reviews Materials 2022

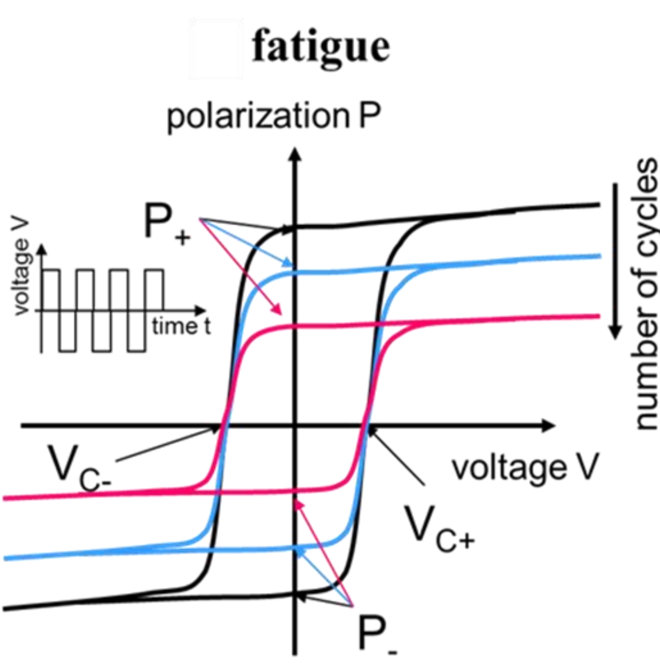
T. Mikolajick et al., IEDM 2019, TED 2020, JAP 2021

	PZT	SBT	PVDF	$X:HfO_2$	AlScN
$2P_R$	~ 30-60µC/cm²	~ 15-30µC/cm²	~ 10-15µC/cm²	~ 30-80µC/cm²	~ 150-250µC/cm²
E_C	~ 0.1 MV/cm	~ 0.05 MV/cm	~ 0.5 MV/cm	~ 1-2 MV/cm	~ 2-5 MV/cm
k	~ 300 – 600	~ 200 – 300	~ 10	~ 30	~ 25
CMOS Comp.	Low to **Medium**	**Low** to Medium	very Low	High	Medium to High Ideal fit to GaN HEMT

Ferroelectrics – Reliability Aspects





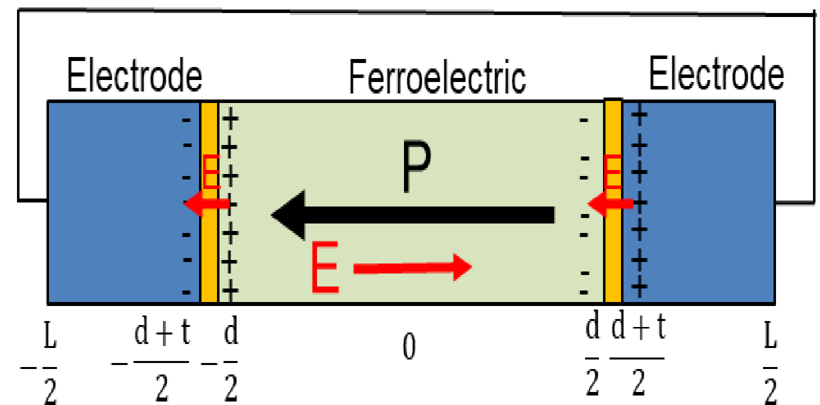


T. Mikolajick, Ref. Mod. in Mat. Sc. and Mat. Eng., Elsevier 2016

T. Mikolajick et al., IRPS 2021

- Retention: Depolarization as a function of time
- Imprint: Parallel shift of hysteresis as a function of time
- Fatigue: Loss of polarization with field cycling
- Wake-up: Increase of polarization with field cycling in the early phase

Ferroelectrics – Depolarization Fields



Depolarization Field

$$E_{FE} = \frac{-Pd_{int}}{\varepsilon_0(d_{int}\varepsilon_{FE} + d_{FE}\varepsilon_{int})}$$

P. D. Lomenzo et al., NVMTS 2019

P. D. Lomenzo et al., ACS Appl. El. Mat. 2020

Top Electrode

Bottom Electrode

Polarization

Non-polar grains

Inter-polar-grain non-polar region

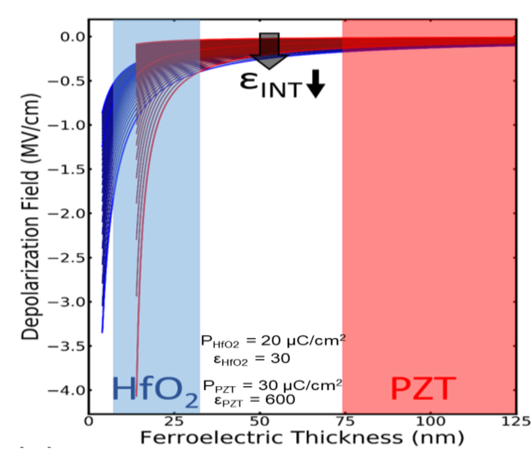
Polar grains

Metal-ferroelectric interface

E_{dep_I}

E_{dep_B}

F. Mehmood et al., Adv. Mat. Interf. 2019



Interface Field

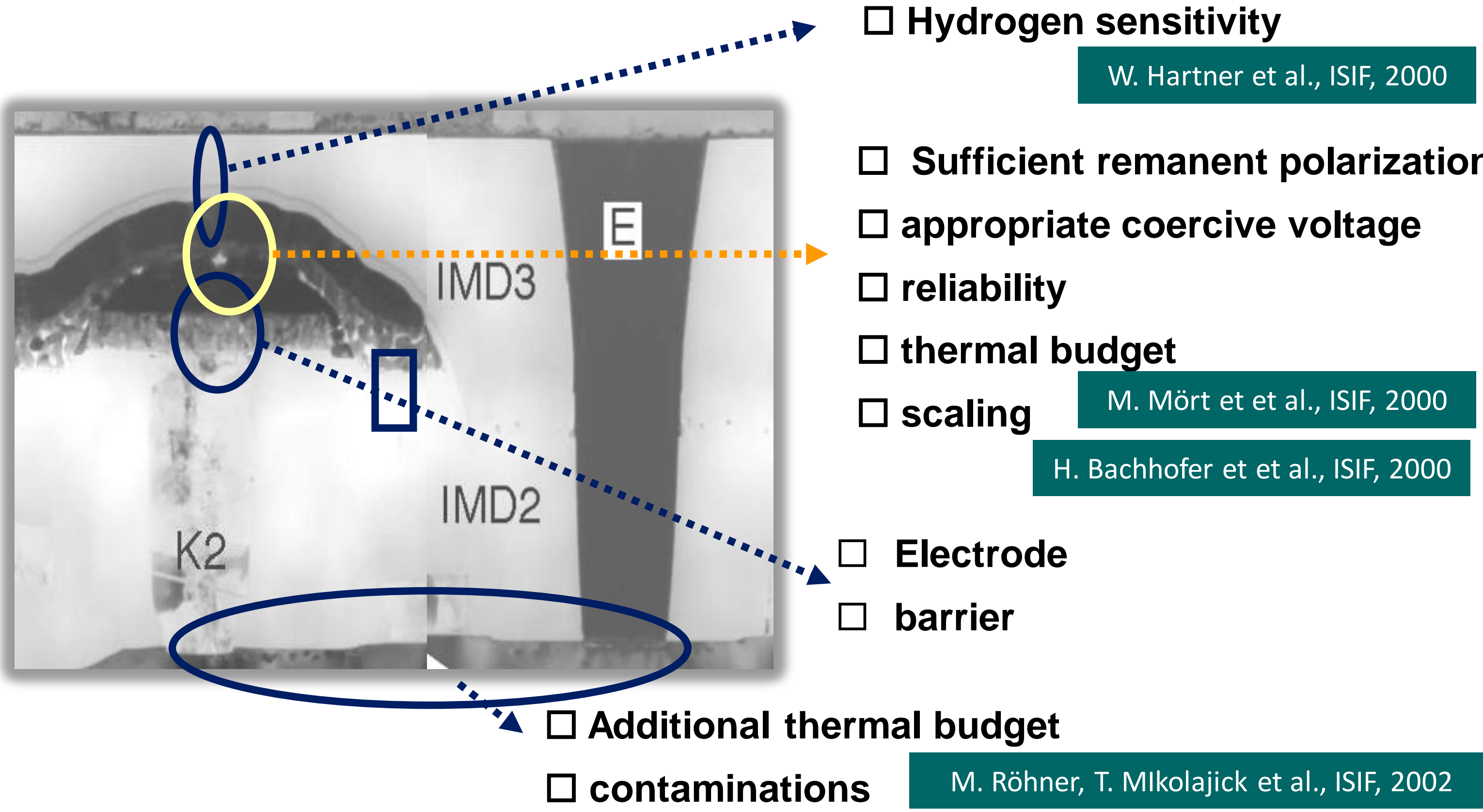
$$E_{INT} = \frac{Pd_{FE}}{\varepsilon_0(d_{int}\varepsilon_{FE} + d_{FE}\varepsilon_{int})}$$

P. D. Lomenzo et al., APL 2020

- Non ideal electrodes and non-polar regions in the ferroelectric lead to a depolarization field
- The depolarization field can lead to a depolarization of the ferroelectric and to charge injection across non-polar interface layers

Ferroelectrics – Integration challenges of perovskites

Material aspects for integration SBT in CMOS



- ☐ Hydrogen sensitivity

W. Hartner et al., ISIF, 2000

- ☐ Sufficient remanent polarization
- ☐ appropriate coercive voltage
- ☐ reliability
- ☐ thermal budget
- ☐ scaling

M. Mört et et al., ISIF, 2000

H. Bachhofer et et al., ISIF, 2000

- ☐ Electrode
- ☐ barrier

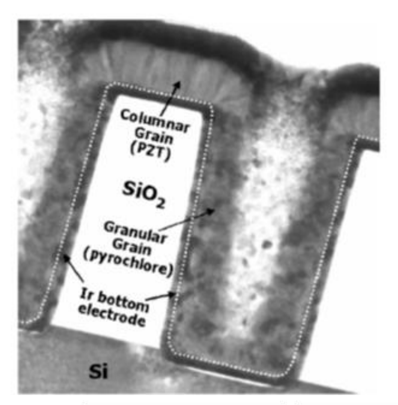
- ☐ Additional thermal budget
- ☐ contaminations

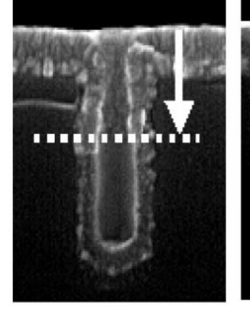
M. Röhner, T. MIkolajick et al., ISIF, 2002

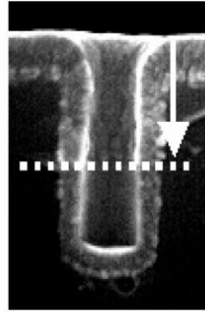
T. MIkolajick et al., Microelectronics Reliability, 2001

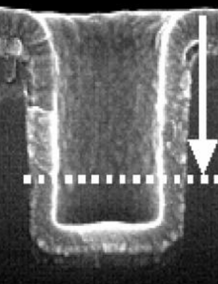
C.-U. Pinnow and T. Mikolajick, Journal of the ECS, 2004

Difficulty of PZT 3D integration







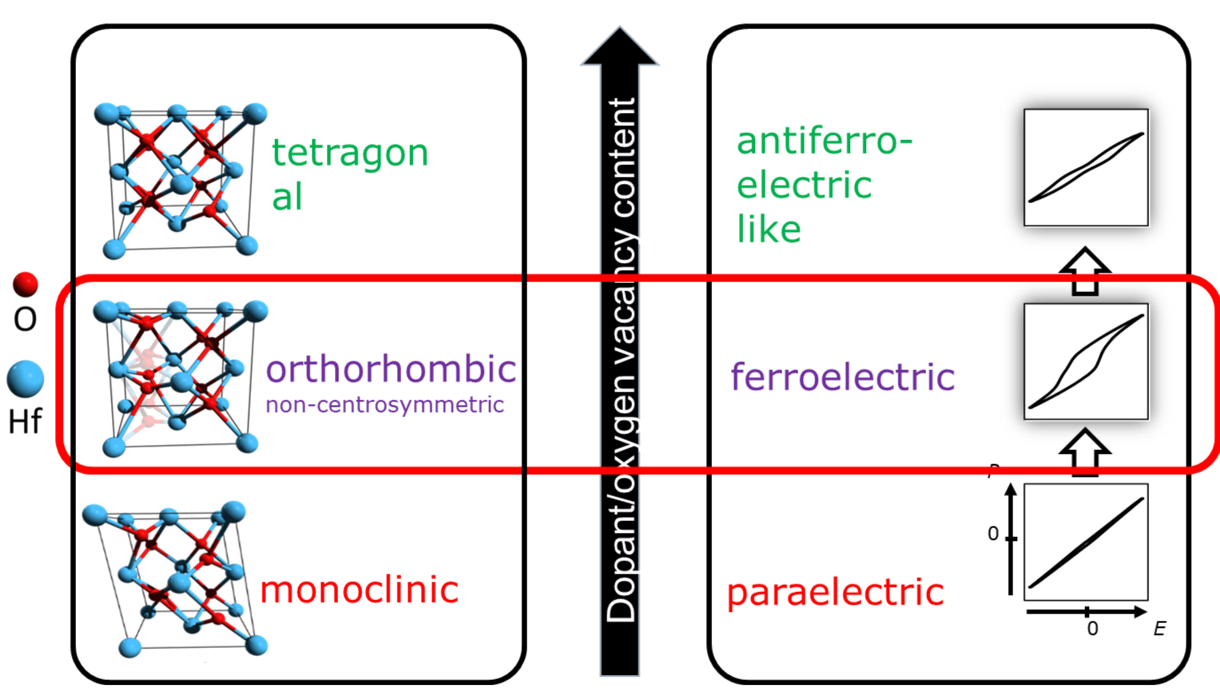


J.-M. Koo et al., IEDM, 2005

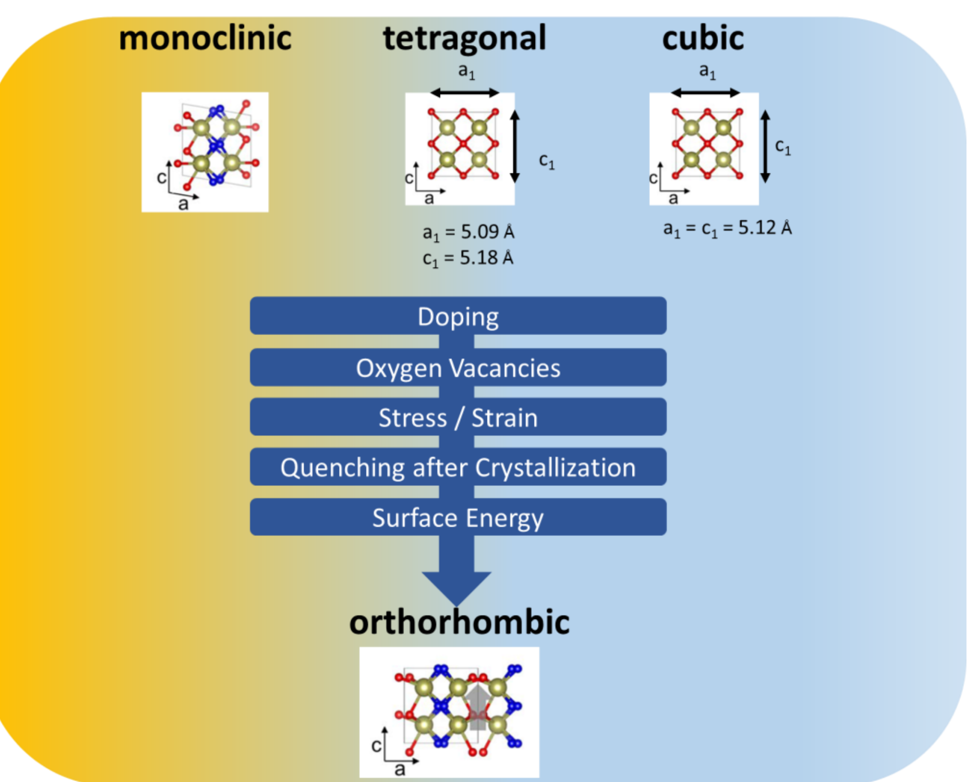
C.-P. Yeh et al., AiP Advances, 2016

Ferroelectrics – Stabilization of the Orthorhombic phase in HfO_2

Polymorphs in polycrystalline hafnium oxide and resulting electrical behavior



Possible knobs to stabilize the orthorhombic phase in HfO_2

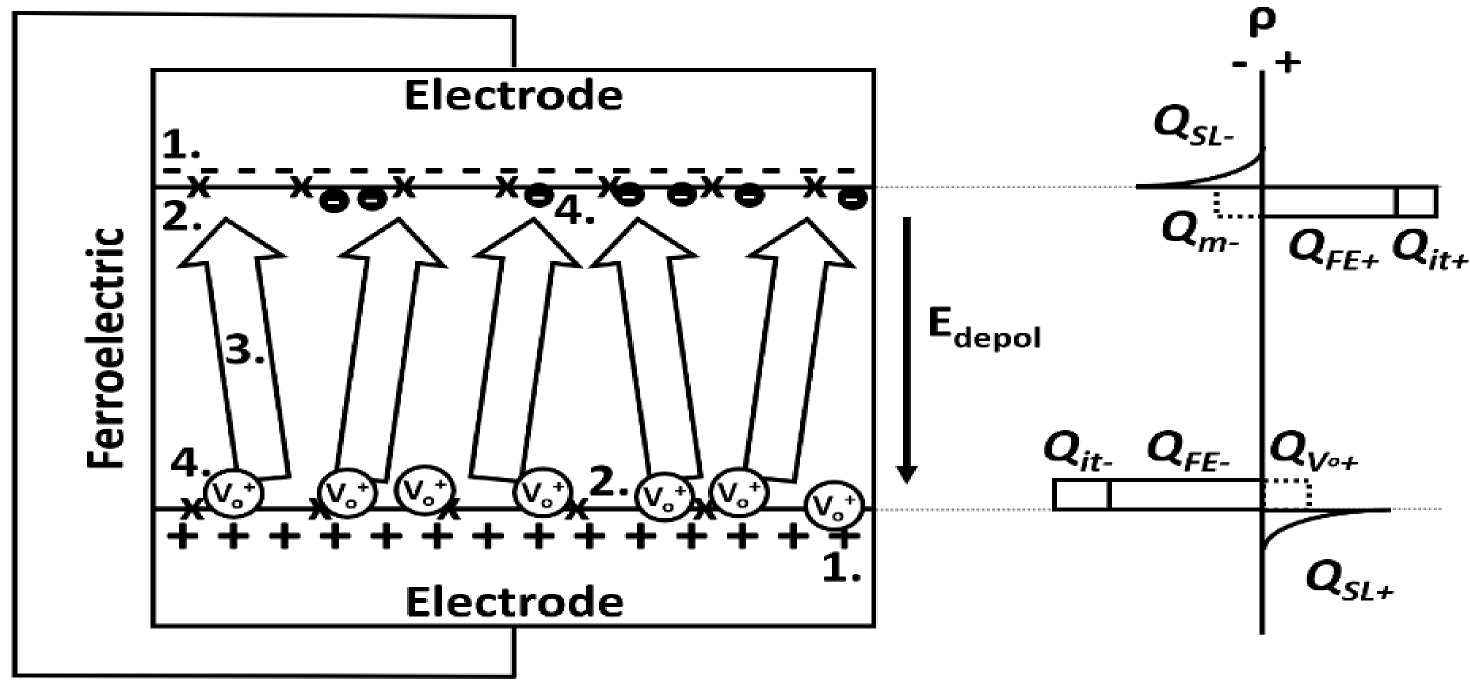


- Orthorhombic HfO_2 is a metastable phase
- Many knobs are know to stabilize the orthorhombic phase
- The different factors involved are interdependent on each other

T. Mikolajick and U. Schröder, Nat. Mat, 2021

Ferroelectrics – Electrode Effects

Ferroelectric capacitor illustrating defects and charges at the electrode/ferroelectric interfaces

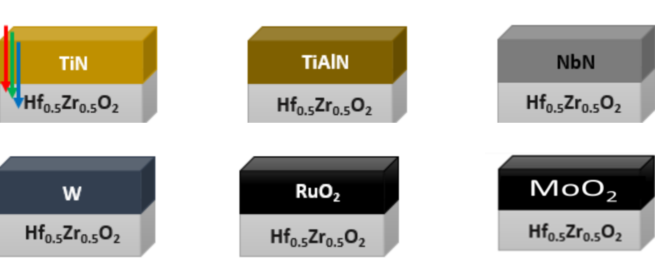


- Interface between electrode and ferroelectric is a highly defective region
- Charge dynamics at the interface is decisive for reliability

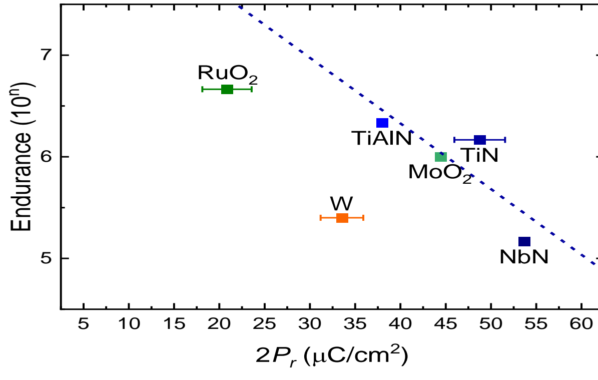
R. Alcala et al., Adv. Funct. Mat. , 2023

Ferroelectrics – Variation of Top Electrode

Investigated Electrodes

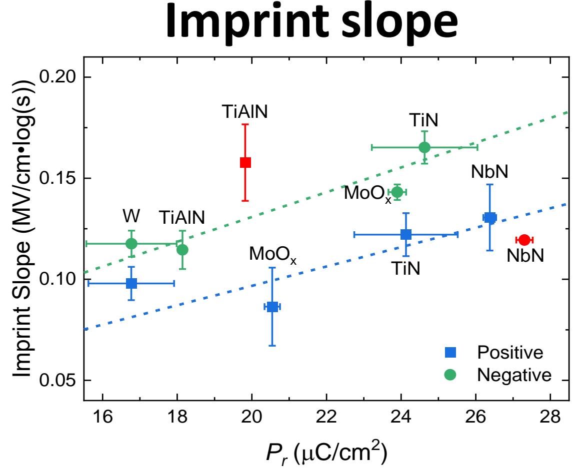


Correlation between Endurance and 2Pr

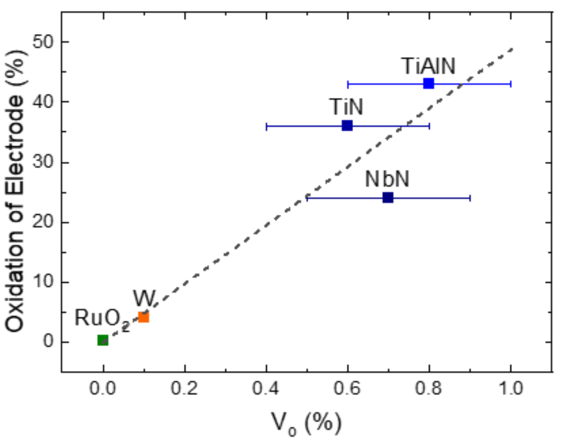


Phase distribution

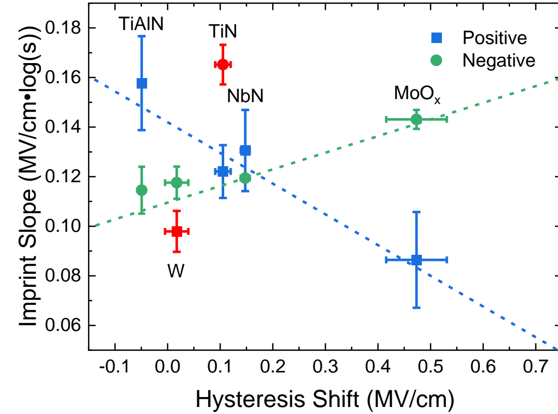
Imprint slope



Estimated oxidation of electrode



Imprint slope vs. Hysteresis shift



R. Alcala et al., Adv. Funct. Mat. , 2023

Ferroelectrics – Variation of Bottom Electrode

Investigated Electrodes

TiN / $Hf_{0.5}Zr_{0.5}O_2$ — W / $Hf_{0.5}Zr_{0.5}O_2$ — MoO_2 / $Hf_{0.5}Zr_{0.5}O_2$

Electrode/HZO lattice mismatch

O-phase fraction vs. 2Pr

Phase distribution

Endurance

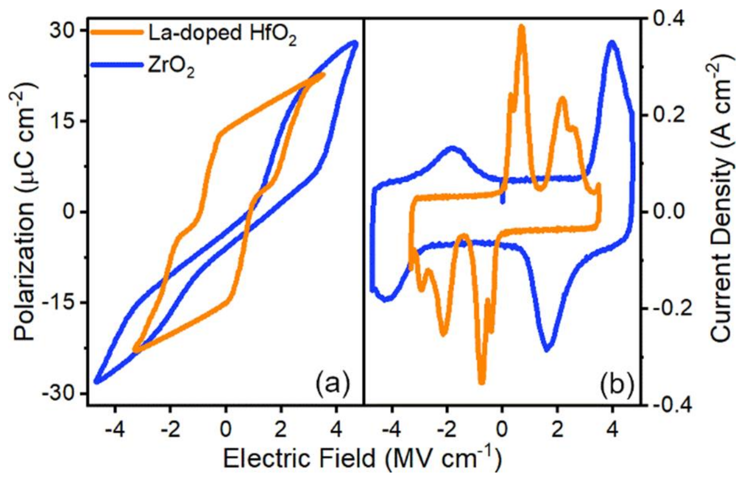
Imprint slope

R. Alcala et al., Adv. Funct. Mat. , 2023

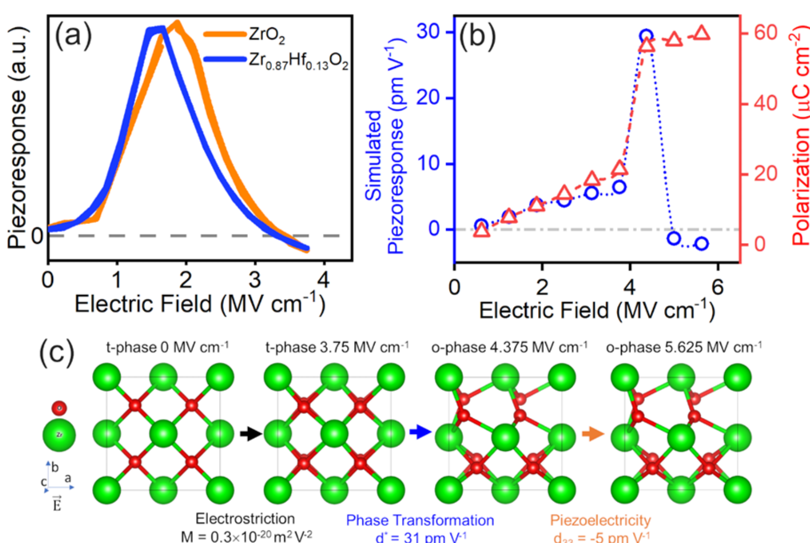
- Phase composition is independent of position of electrode (top or bottom)
- Reduced scavenging of oxide and nitride electrode leads to increased m-phase and reduce polarization
- Tensile stress (large lattice parameter ratio between electrode and HZO, is more effectively increases Pr at the BE
- No pronounced effect on reliability

Ferroelectrics – Origin of Antiferroelectric Hysteresis

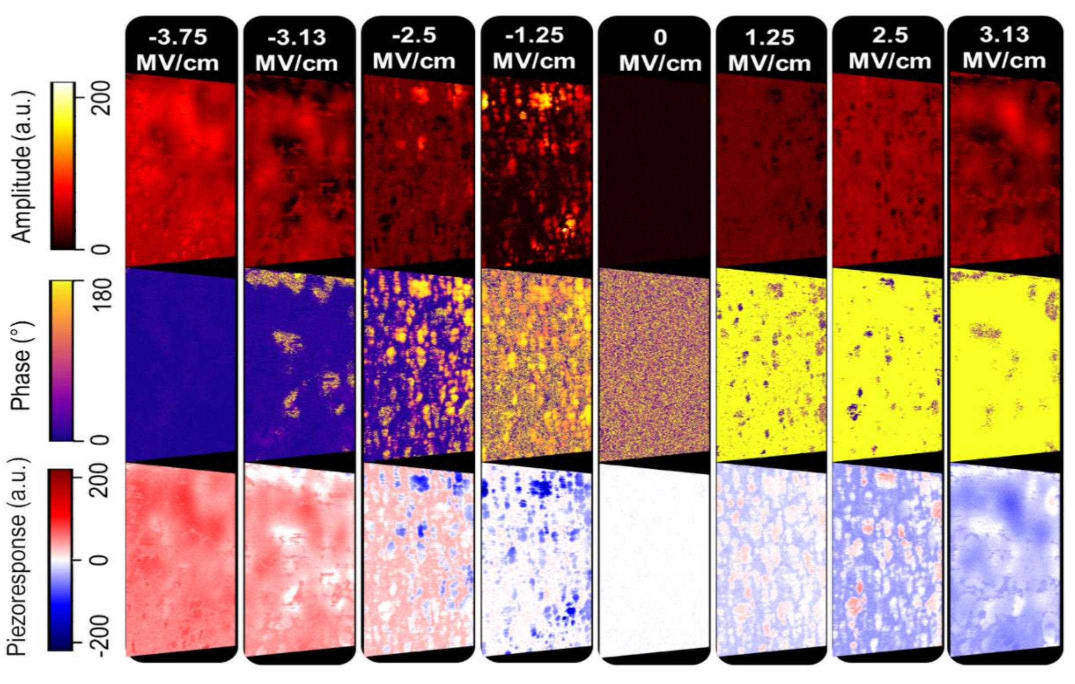
Antiferroelectric hysteresis vs. antiferroelectric like hysteresis



Simulated and measured piezoresponse



Direct observation of field induced phase transition using Band Excitation (BE) AFM



P. D. Lomenzo et all., Adv. Funk. Mat., 2023

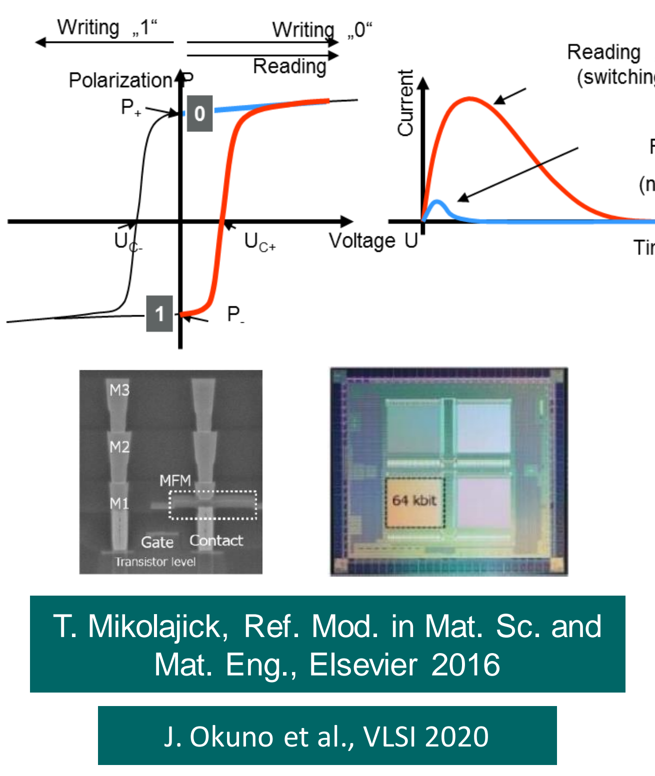
- Origin of antiferroelectric hysteresis is still not 100% clarified
- On hypothesis is a field induced phase transformation
- Direct experimental evidence for the field induced phase transformation is achieved by BE-AFM

Outline

- Introduction
- Ferroelectric Materials for Semiconductor Devices
- Basic Ferroelectric Memory Devices
- Ferroelectric enhanced Devices for Beyond von-Neumann Computing
- Ferroelectric Devices for other Applications
- Summary and Conclusion

Basic Ferroelectric Memory Device – Overview

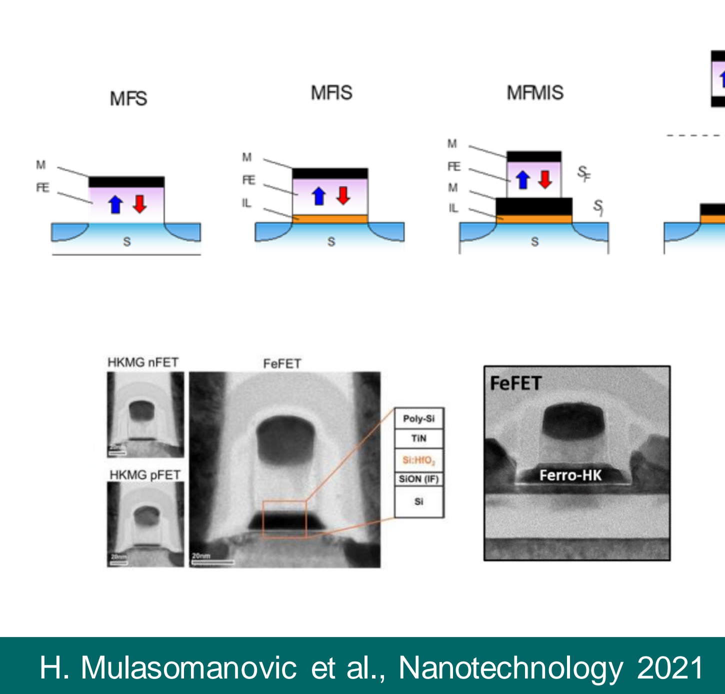
Readout by switched charge: FeRAM (DRAM like)



T. Mikolajick, Ref. Mod. in Mat. Sc. and Mat. Eng., Elsevier 2016

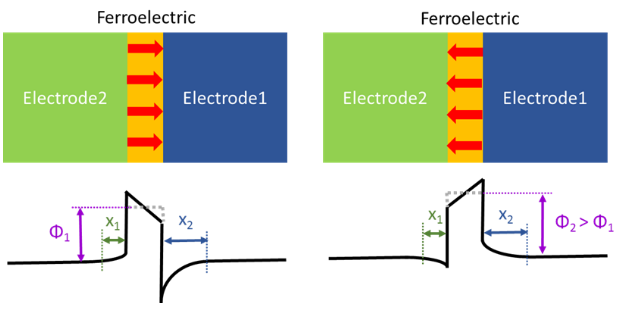
J. Okuno et al., VLSI 2020

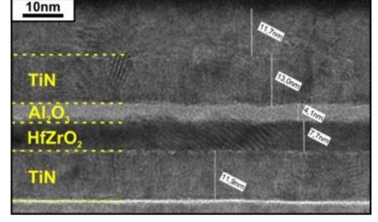
Readout by coupling to transistor channel: FeFET (Flash like)



H. Mulasomanovic et al., Nanotechnology 2021

Readout by resistance change: FTJ (RRAM like)





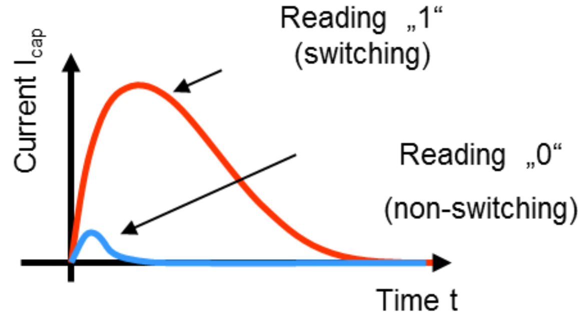
E. Y. Tsymbal and H. Kohlstedt, Science 2006

B. Max et al., JEDS 2019

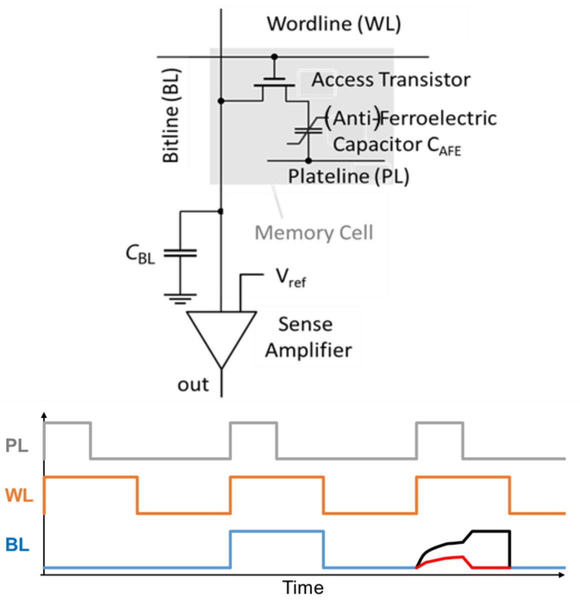
- Ferroelectric materials enable three fundamentally different types of memory devices
- New possibilities for in-memory computing and neuromorphic computing

Basic Ferroelectric Memory Devices – FeRAM

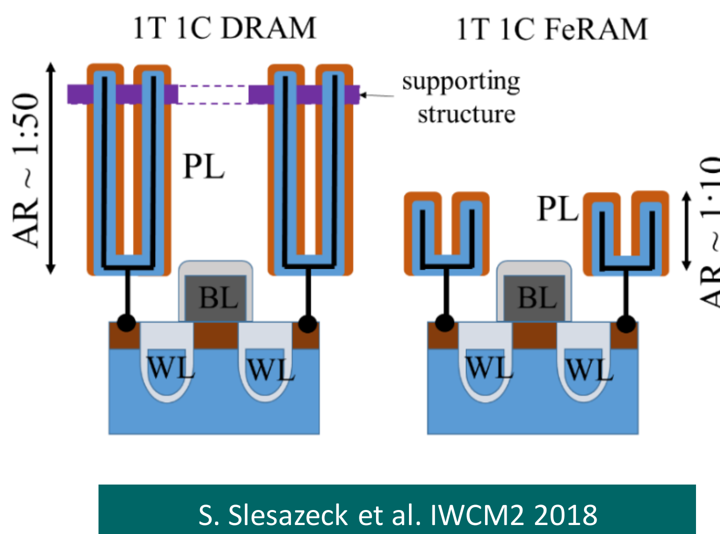
Curent reponse during reading out of a capacitor



Readout in 1T-1C FeRAM cell



Comparison of stacked capacitor height between DRAM and HfO_2 based FeRAM

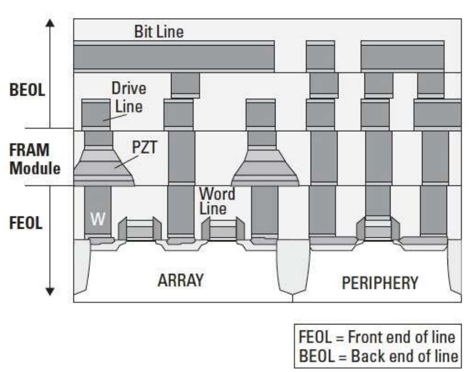


S. Slesazeck et al. IWCM2 2018

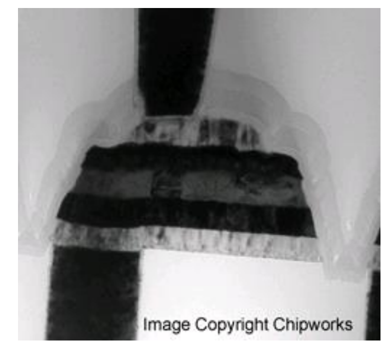
- For readout a pulse in a defined direction is applied to the capacitor
- If the ferroelectric does not switch then only the displacement current will flow
- If the ferroelectric switches, then in addition to the displacement current the switching current will flow
- Switched charge needs to be high enough to develop a reasonable voltage on the bitline

Basic Ferroelectric Memory Devices – FeRAM

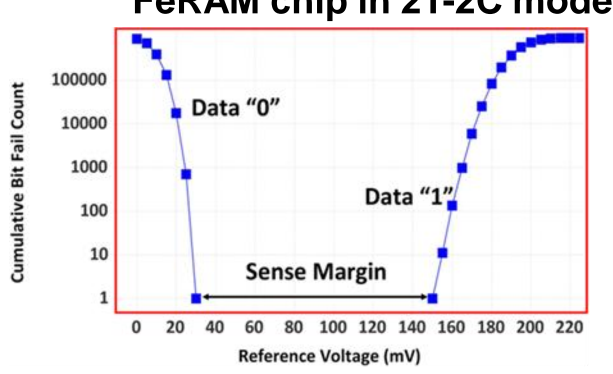
Schematic cross section of 130nm PZT FeRAM



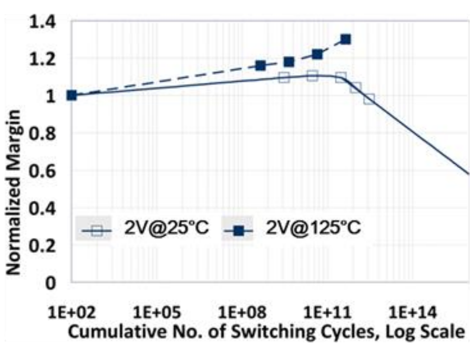
TEM Cross section of PZT FeRAM capacitor



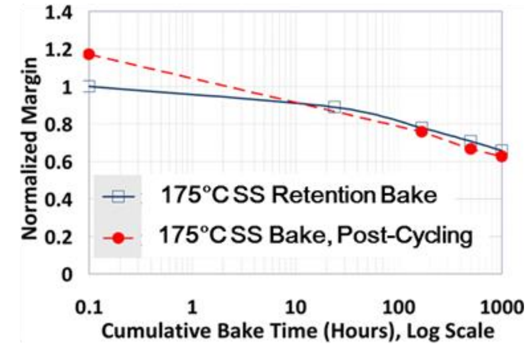
Bit distribution for 180nm PZT FeRAM chip in 2T-2C mode



Enduracnce of 180nm PZT FeRAM chip in 2T-2C mode



Retention test for 180nm FeRAM chip in 2T-2C mode with and without pre-cycling

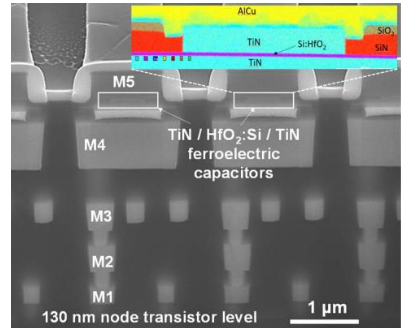


- First ferroelectric memories came to market in the early 1990s
- Today state of the art is 130nm/90nm technology
- Very good performance and reliability data

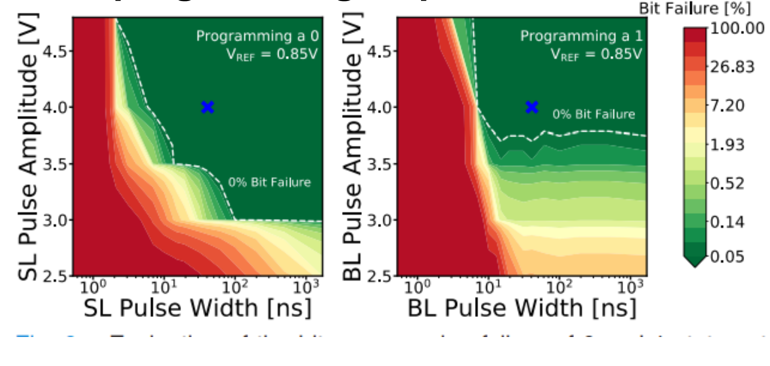
K. R. Udayakumar et al., IMW 2013

Basic Ferroelectric Memory Devices – FeRAM

SEM of HZO based FeRAM cells integrated in 130nm CMOS



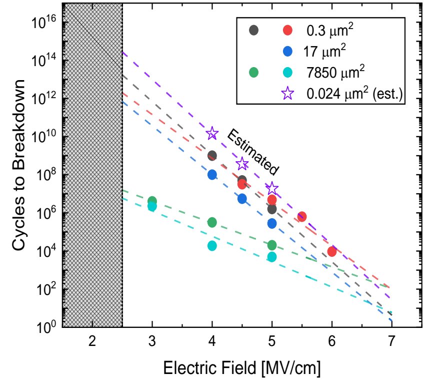
Bit failures as a function of programming amplitude



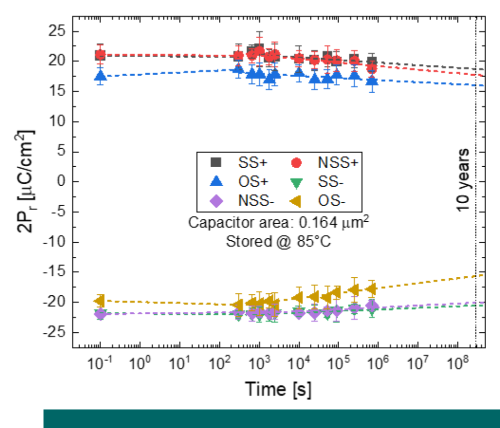
T. Francois et al., IEDM 2019, 2021

T. Francois et al., TED 2022

Field dependent Endurance of MFM capacitor with Si-doped HfO_2 for different capacitor sizes

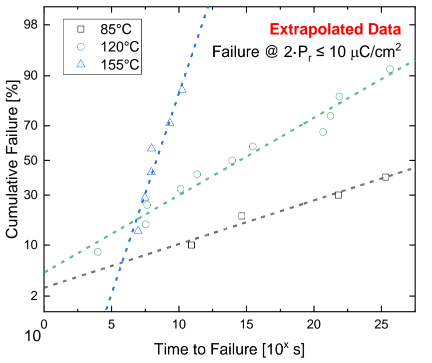


Retention of MFM capacitor with Si-doped HfO_2 for different capacitor sizes



R. Alcala et al., EDTM 2022

Extrapolated retention failure rate for different temperatures



Influence of area, Temp and Field on reliability of MFM capacitor with Si-doped HfO_2

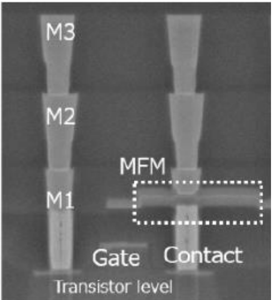
	Wake-Up	Cycles to Break.	Imprint	Retention
Area (↓)	-	↑	-	-
Temperature (↓)			↓	↑
Electric Field (↓)	-	↑		

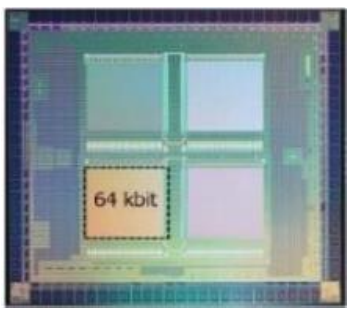
R. Alcala et al., JEDS 2022

- Promising data for integrated FeRAM using silicon doped hafnium oxide has been shown

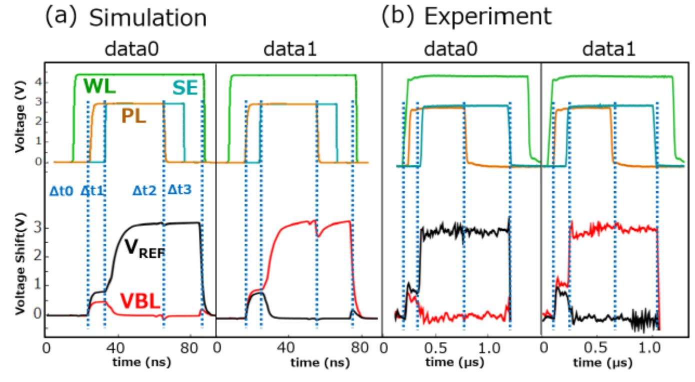
Basic Ferroelectric Memory Devices – FeRAM

Cross section of cell and top view of 64kbit 1T-1C HZO FeRAM

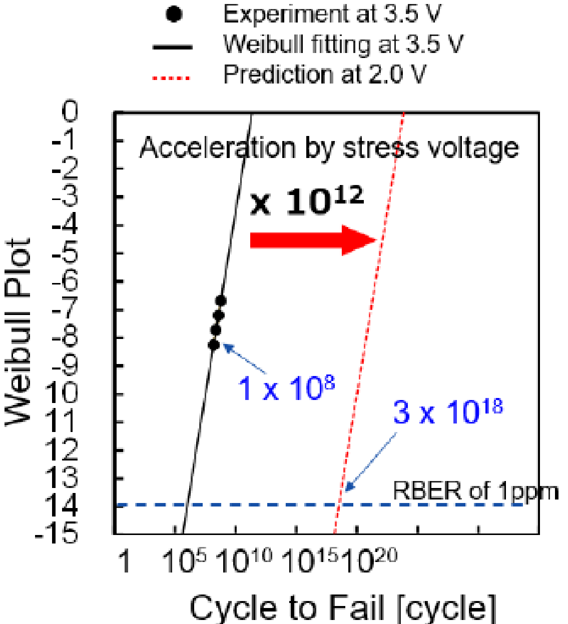




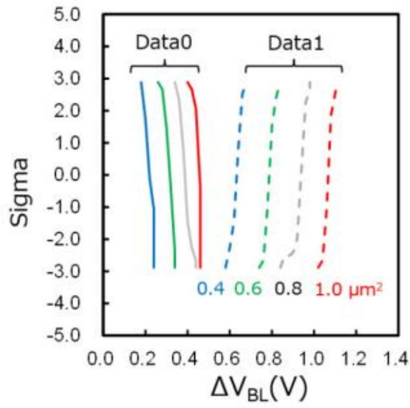
Simulated and measured read operation of 1T-1C HZO FeRAM



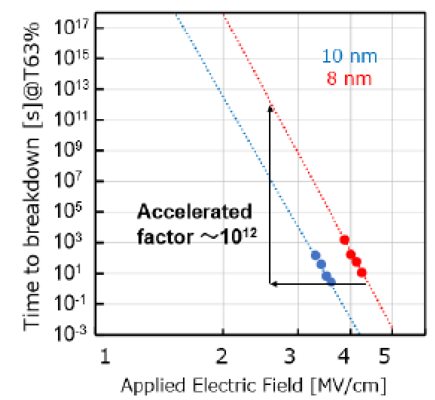
Weibull plot of the cycling failures measured and extrapolated for a 8nm thick HZO film



V_{BL} distribution of 1T1C HZO FeRAM for different capacitor sizes



Time to breakdown for HZO as a function of electric field and film thickness



J. Okuno et al., VLSI 2020

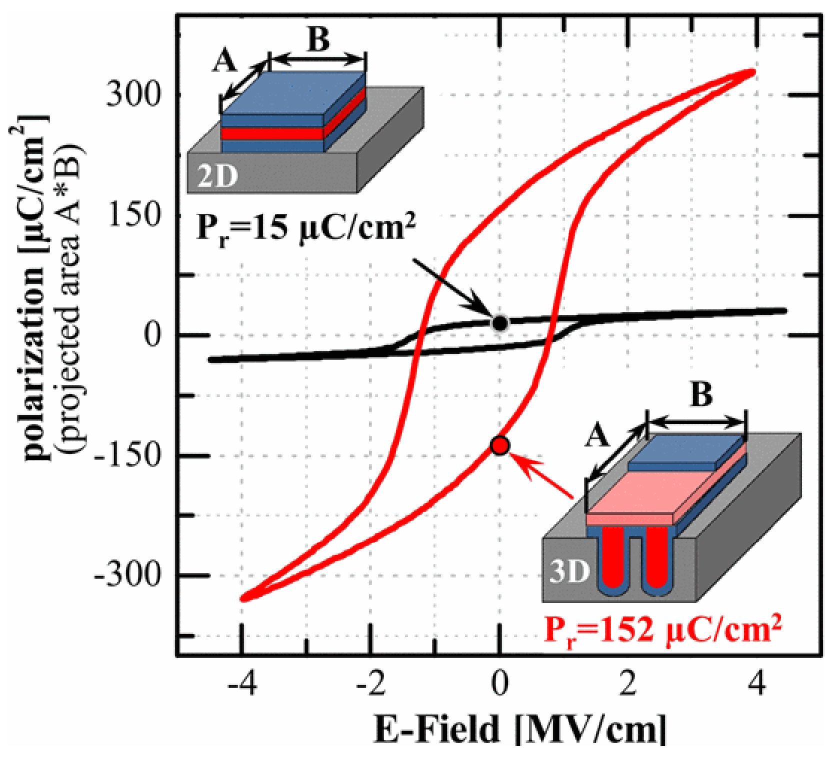
J. Okuno et al., JEDS 2022

J. Okuno et al., EDTM 2022

- First promising data for integrated FeRAM using HZO has been shown

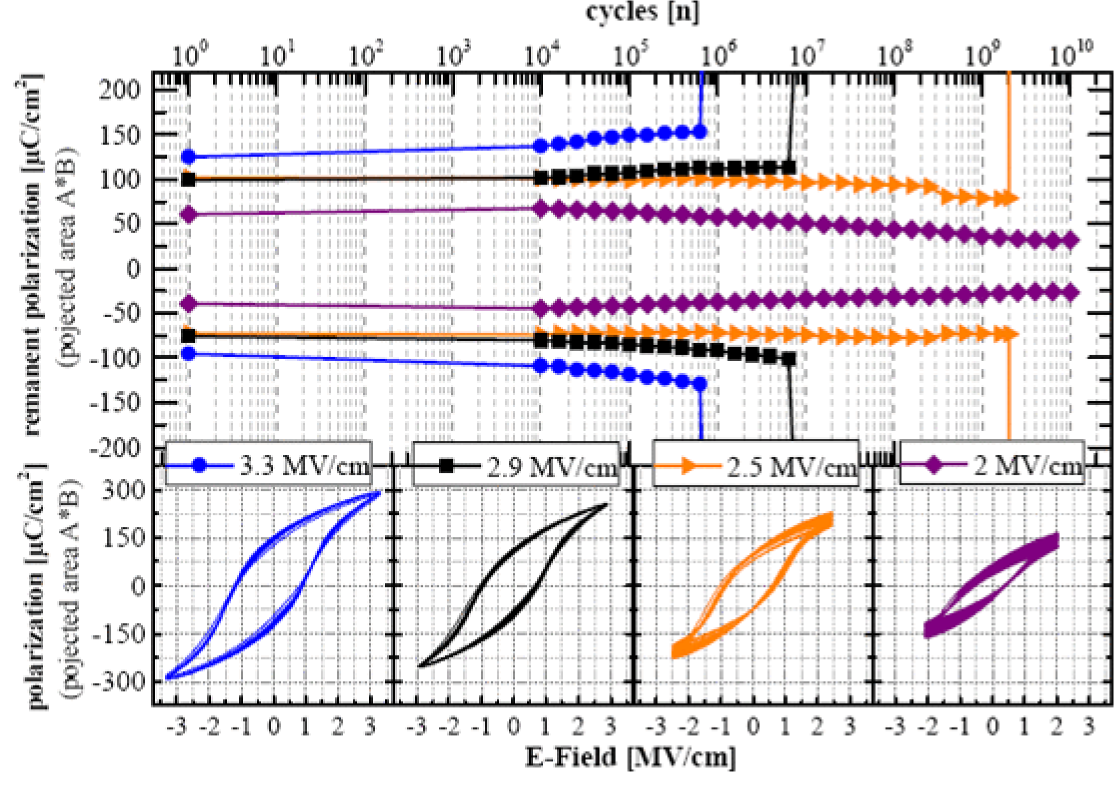
Basic Ferroelectric Memory Devices – FeRAM

Polarization per footprint of 2D and 3D structure



J. Müller et al., IEDM 2013

Endurance of 3D structures for different cycling fields

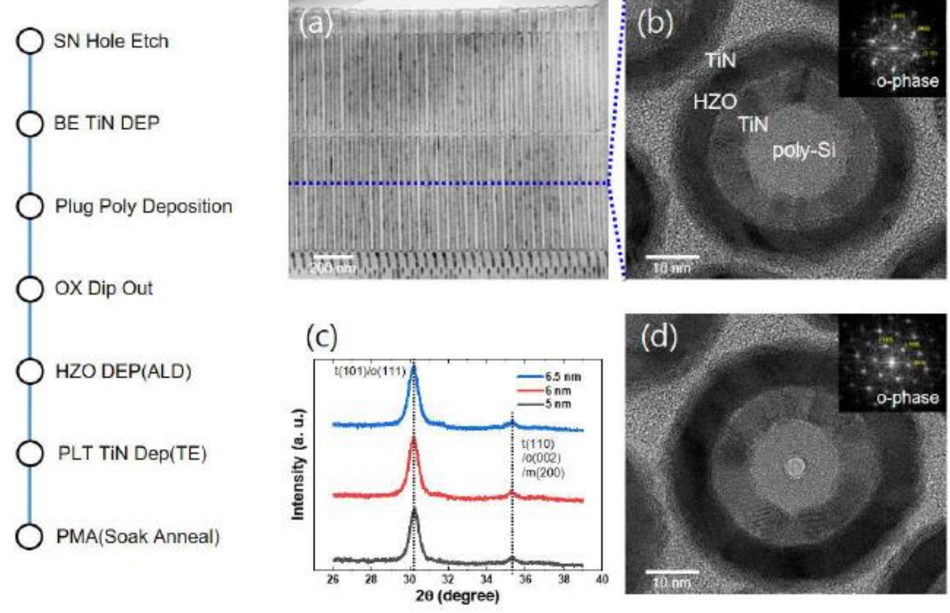


P. Polakowski, IMW 2014

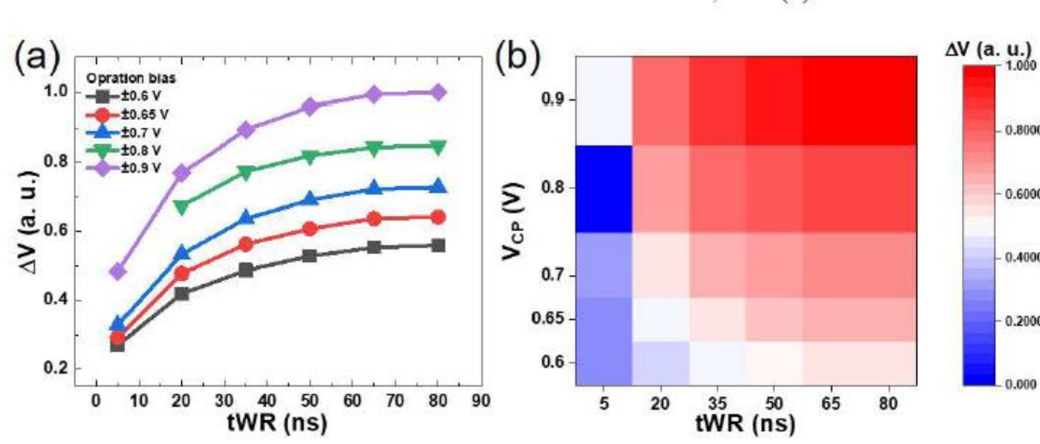
- 3D integration is straight forward based on available ALD processes

Basic Ferroelectric Memory Devices – FeRAM

Process flow, cross vertical and top-view cross sections as well as XRD pattern for 5nm and 7nm HZO integrated into 1xnm technology



Characterization of writing process in 1xnm HZO based FeRAM

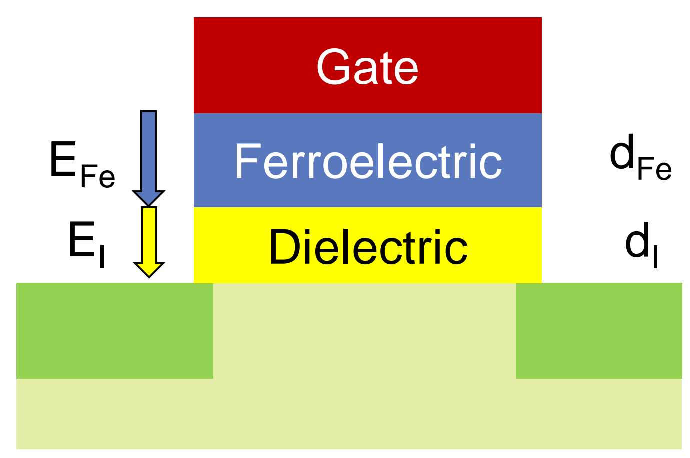


- First demonstration of HZO integration into 1xnm technology
- Little data publicly available so far

M. Sung et al., IEDM 2021

Basic Ferroelectric Memory Devices – FeFET - reminder

Generic ferroelectric FET



Gate voltage

$$V_G = \varphi_S + \frac{Q_{SC}(\varphi_S)}{C_{Stack}} + E_{Fe} \cdot d_{Fe}$$

At flatband

$$V_{FB} = E_{Fe}(P = 0) \cdot d_{Fe}$$

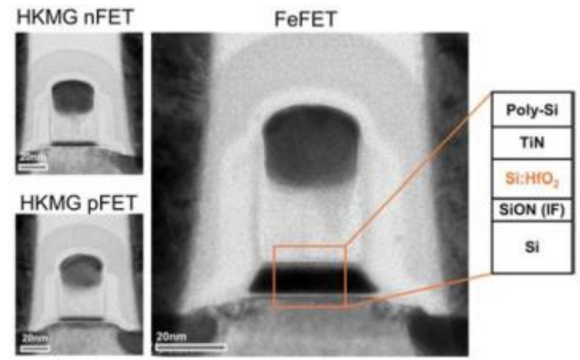
Memory window

$$MW = V_{FB+} - V_{FB-} \approx 2 \cdot E_C \cdot d_{Fe}$$

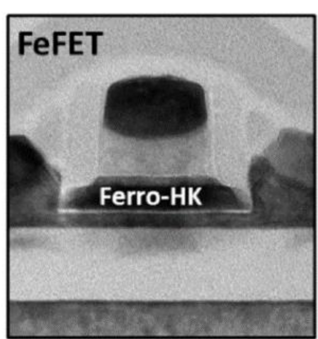
- Qsc is the space charge in the silicon and C_{stack} is the capacitance of the series connection of ferroelectric and dielectric capacitor (assumption: No trapped or fixed charge)
- The nonlinear and switching behavior of the ferroelectric as a function of the electrical field modifies the I-V characteristics of a FeFET compared to a normal MOSFET
- The ferroelectric switching leads to hysteresis
- The memory window depends on the coercive field and the thickness of the material

Basic Ferroelectric Memory Devices – FeFET

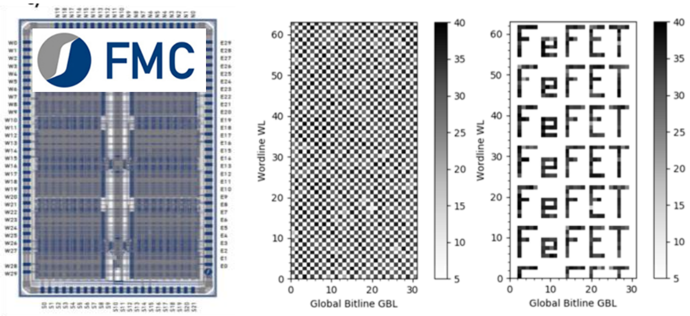
Cross sections of 28nm logic FETs and FeFET



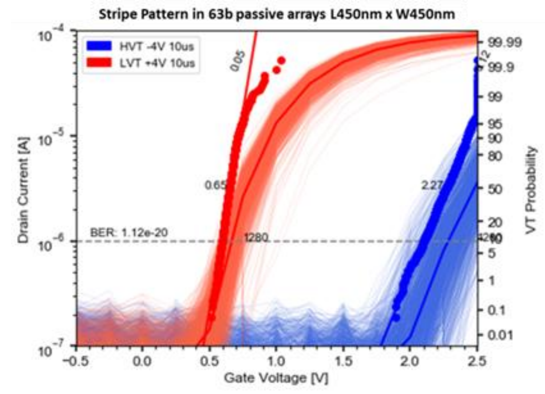
22nm FDSOI FeFET device



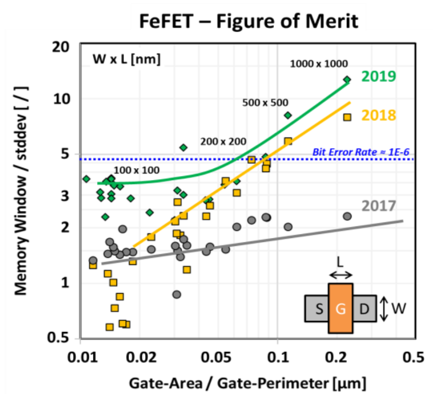
10MbArray
Layout and test patterns



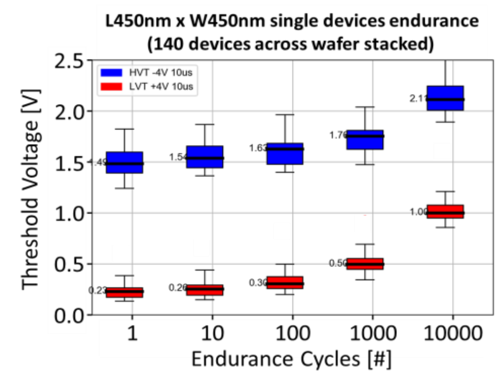
I-V curves for low and high VT states of 28nm FeFET device across



Improvement of Variability over time



Cycling endurance behavior



M. Trentzsch et al., IEDM 2016

S. Dünkel et al., IEDM 2017

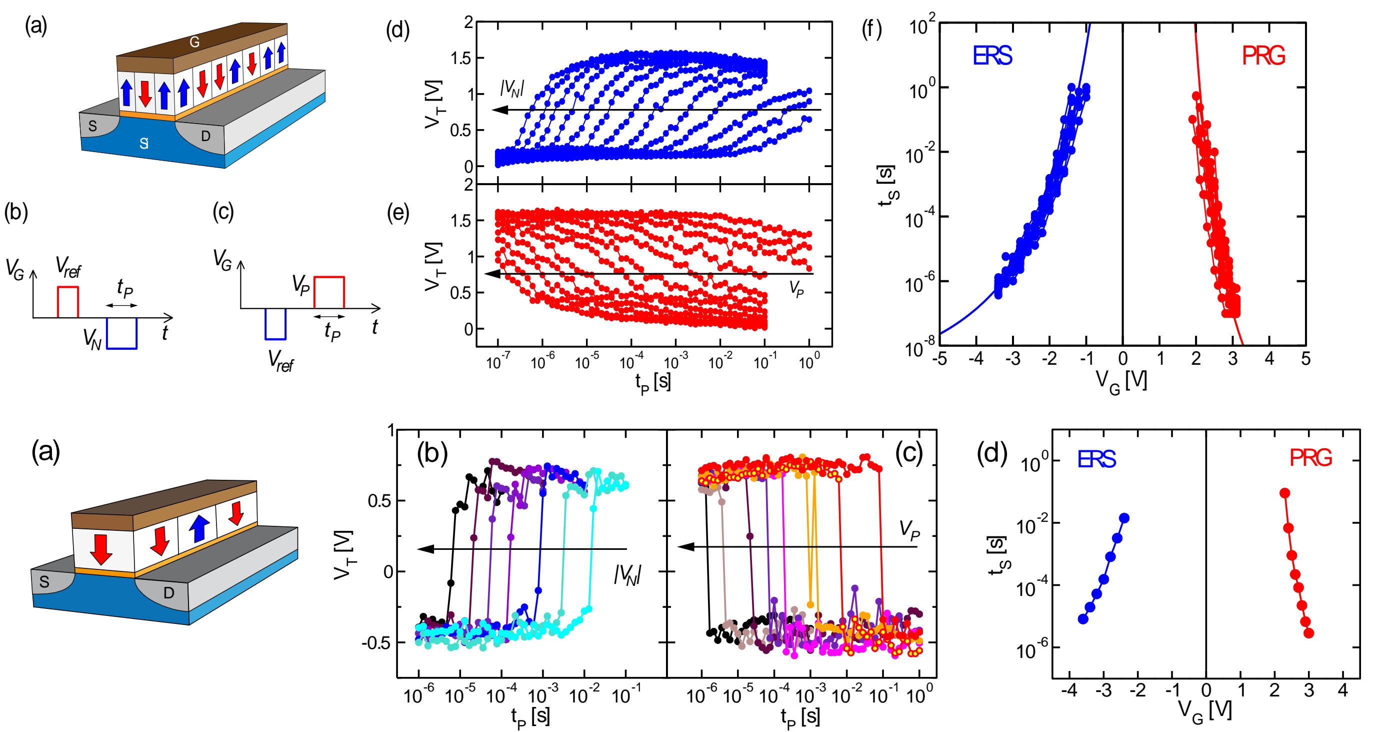
S. Beyer et al., IMW 2020

H. Mulasomanovic et al., Nanotechnology 2021

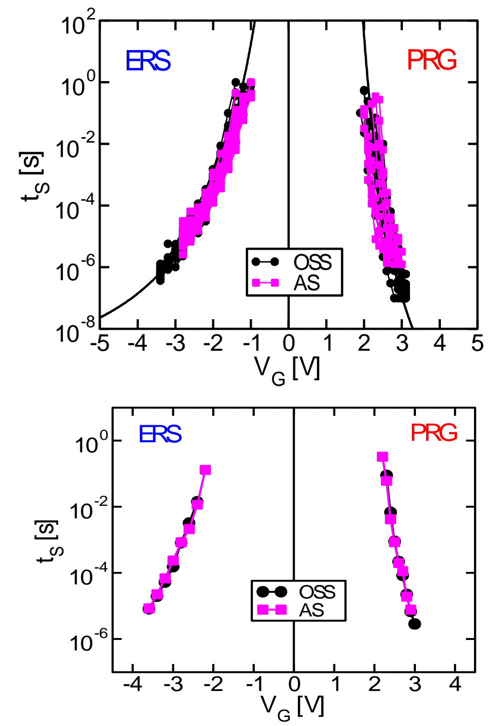
- Cell transistor only differs in HfO_2 details; Periphery devices not affected
- Array is fully functional and variability is continuously improving

Ferroelectric Memories – FeFET

Construction of VG vs. ts plots using one shot switching in large and small devices



Comparison of accumulative switching (AS) and one shot switching (OSS) in large and small devices

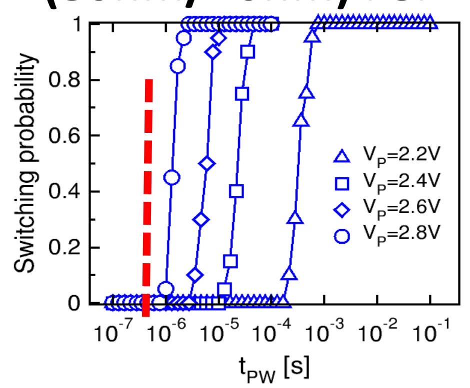


- VG vs. t_s plot can be used to extract retention behavior form switching experiments
- Switching in large and small devices is continuous vs. abrupt
- VG vs. t_s behavior is universal for large and small devices using one shot and accumulative switching

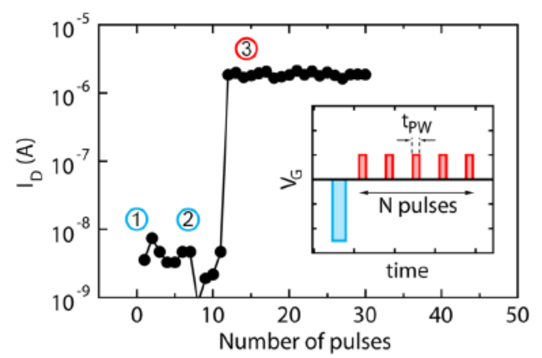
H. Mulaosmanovic et al., TED 2020

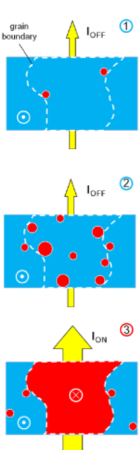
Ferroelectric Memories – FeFET

Switching probability of scaled (80nm/20nm) FeFET

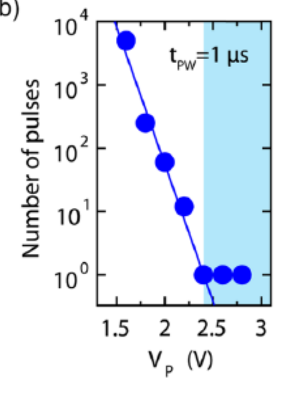


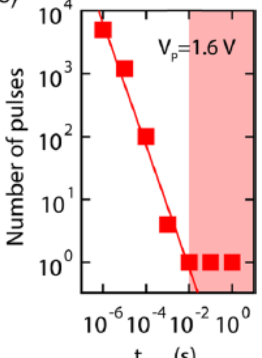
Accumulative switching of scaled FeFET





Number of pulses required to switch scaled FeFET as a function of pulse height and width





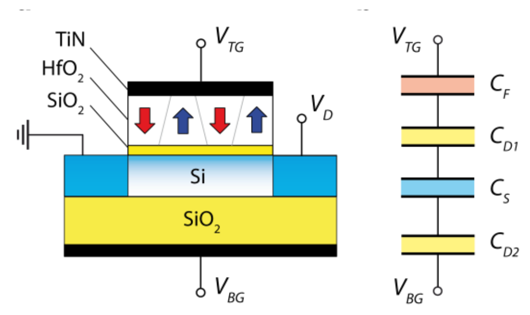
- Ultra-scaled FeFETs exhibit accumulative switching
- Probability curve is tunable
- The effect can be used for mimicking biological neurons

H. Mulaosmanovic et al., ACS AMI 2018

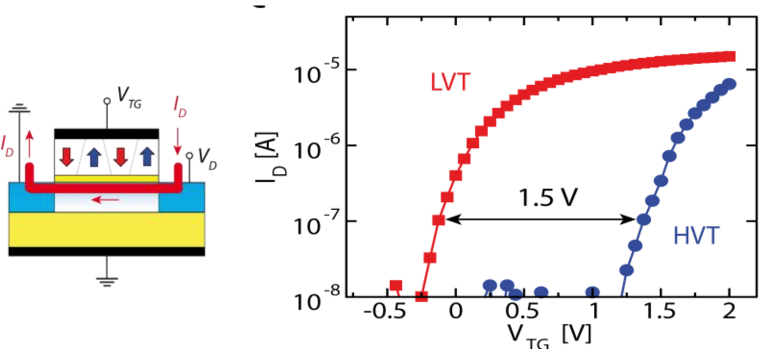
H. Mulaosmanovic et al., Nanoscale 2018

Ferroelectric Memories – FeFET

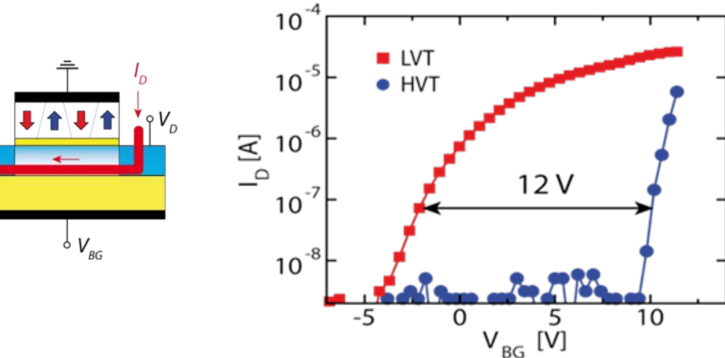
FDSOI FeFET illustrating front- and back-gate capacitances



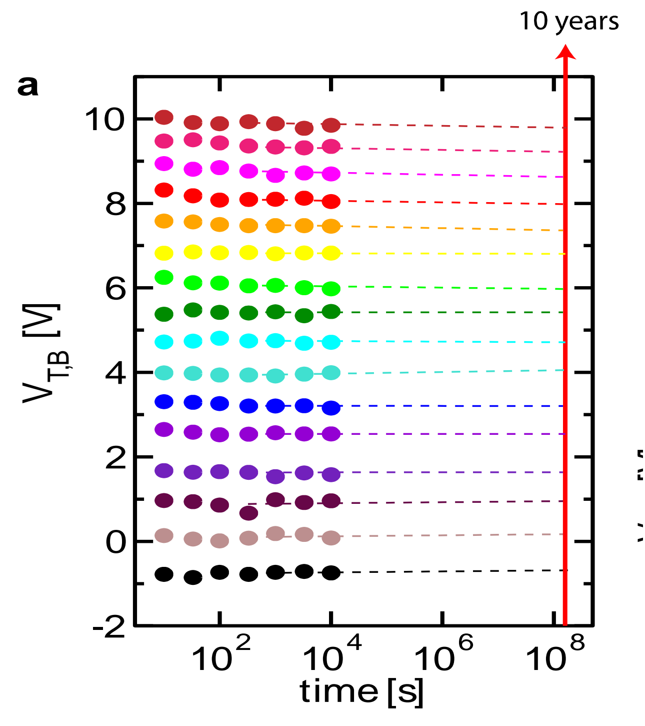
Reading from front-gate



Reading from back-gate



Demonstration of 8-V_T levels

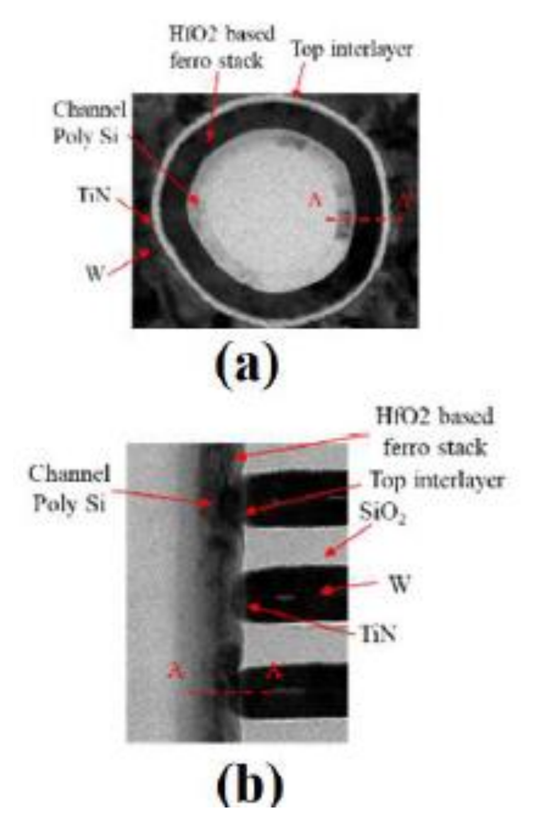


H. Mulaosmanovic et al., Nanoscale 2021

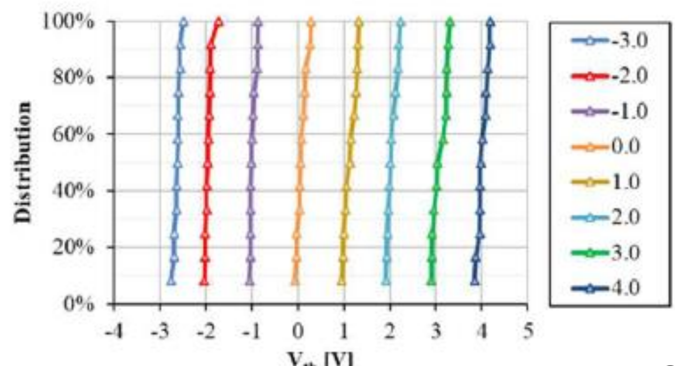
- With two different gates, the write and read paths of a FeFET can be decoupled
- With a significantly thicker gate dielectric in between second gate and channel, the read signal is amplified
- One possible implementation can be achieved by using the back-gate of an FDSOI device

Ferroelectric Memories – FeFET

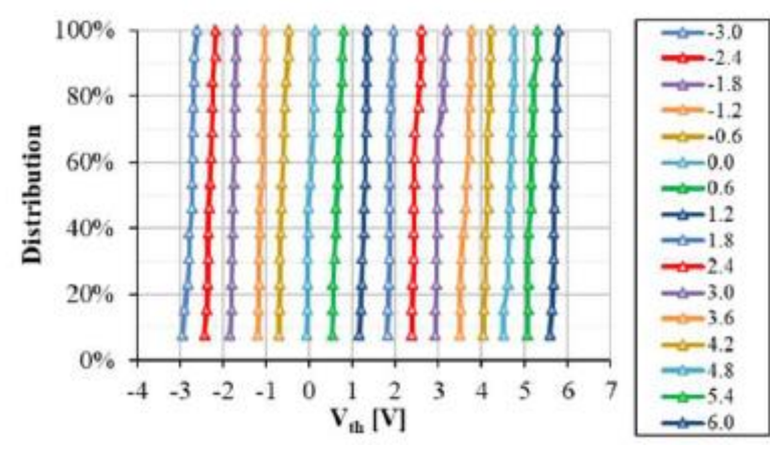
FeFET integrated into 3D NAND



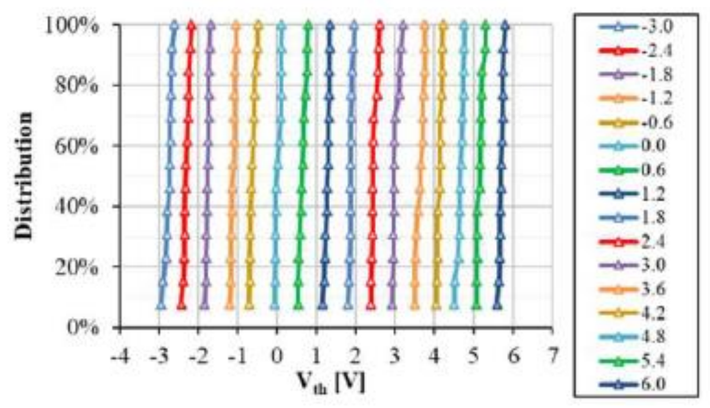
Cell distributions for 3bits per cell



Cell distributions for 4bits per cell



Cell distributions for 4 bits per cell after 3k cycles

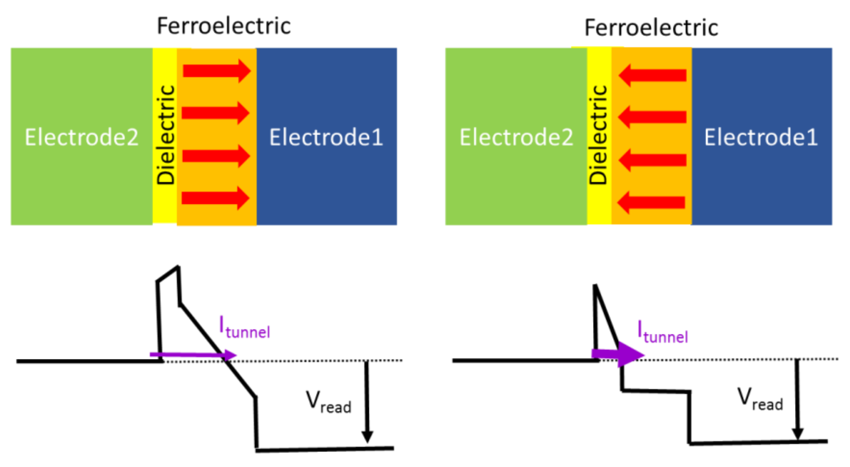


- First data on integration of ferroelectric Hafnia into 3D NAND shows promising data even for 3 - 4 bits/cell operation

S. Yoon et al. , VLSI 2023

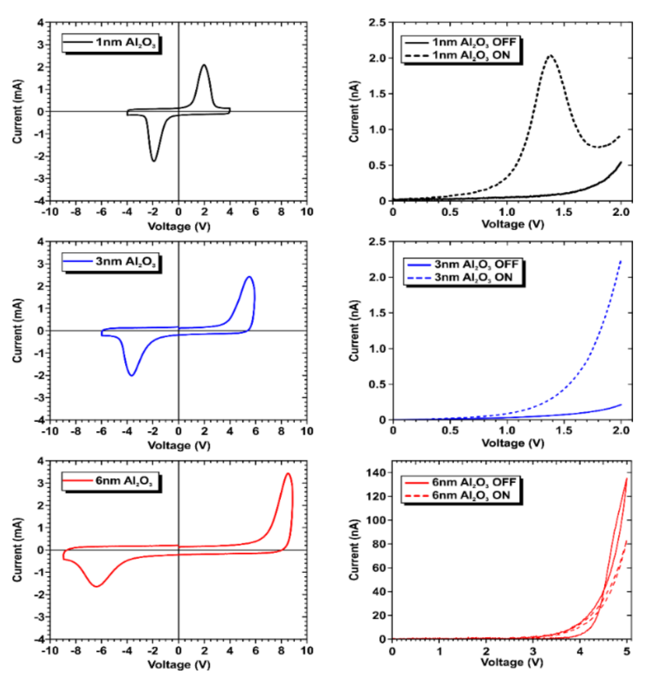
Ferroelectric Memories – FTJ

Two Layer Ferroelectric Tunnel Junction



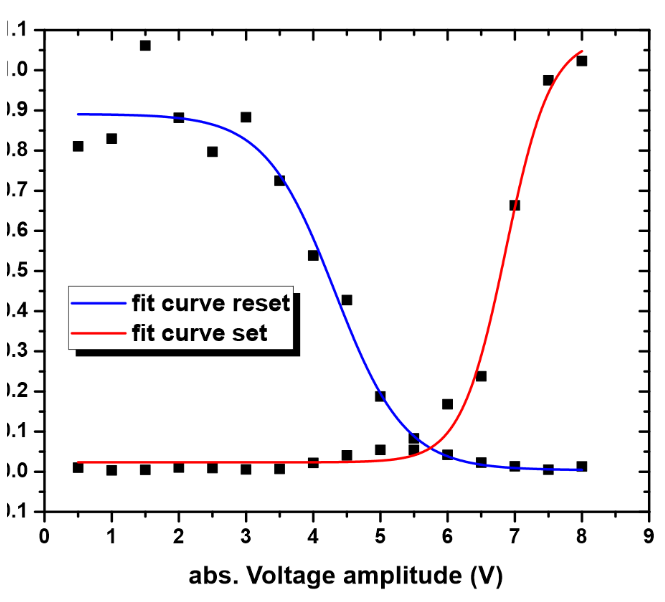
B. Max et al., ESSDERC 2018

Switching and reading behavior of two layer FTJ using 1nm, 3nm and 6nm tunneling layer



B. Max et al., JEDS 2019

Fraction of switched area as a function of pulse amplitude

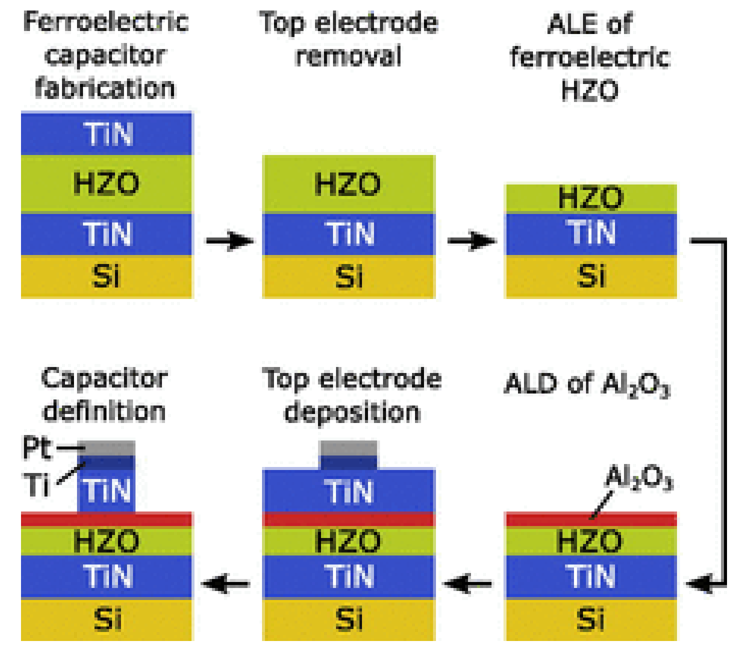


B. Max et al., ACS Appl. El . Mat, 2020

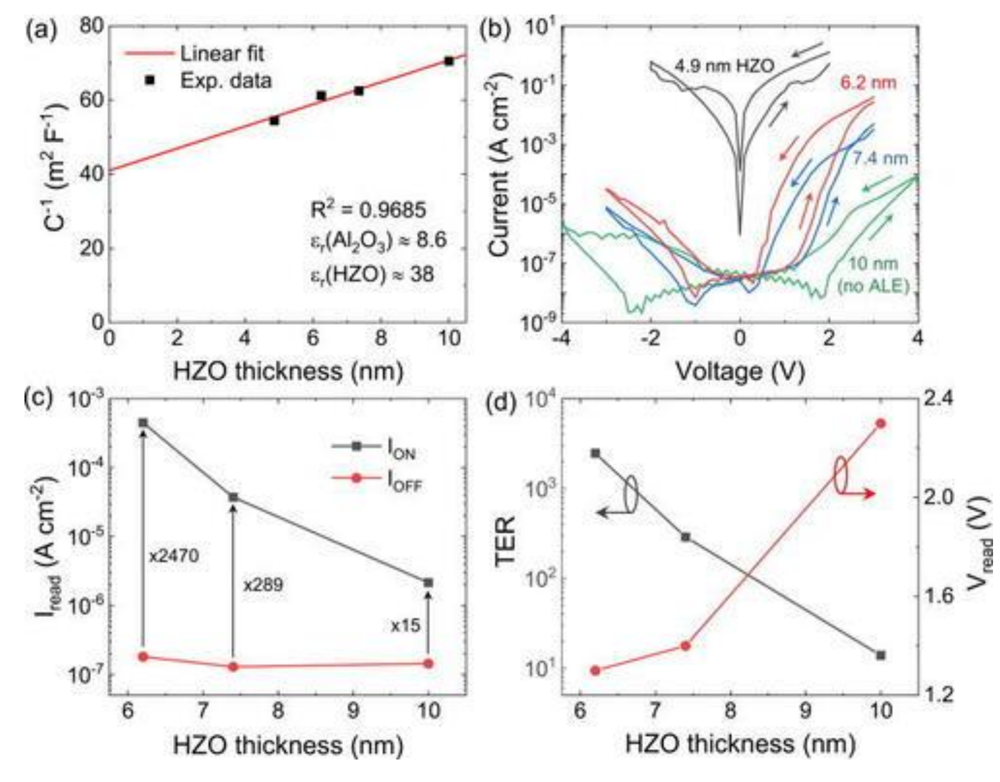
- FTJ is a two terminal resistive switching device
- Stable device operation is possible in a certain thickness window; Dependent on material choice
- Multi-Level is demonstrated in large area test structure

Ferroelectric Memories – FTJ

Thinning of ferroelectric layer using atomic layer etching



FTJ performance with thinned HZO layer



M. Hoffmann et al., APL 2022

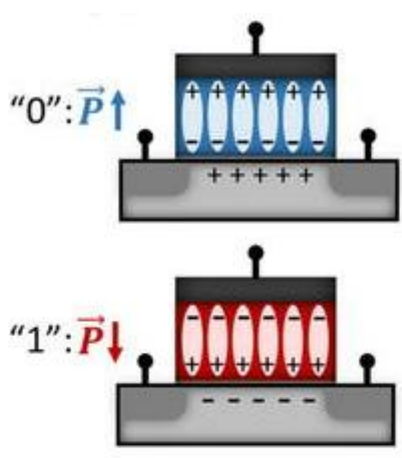
- Low current is the biggest issue in FTJ devices
- Hafnium Oxide with a thickness below 8nm is hard to stabilize in the orthorhombic phase
- Thinning after the crystallization can be an alternative

Outline

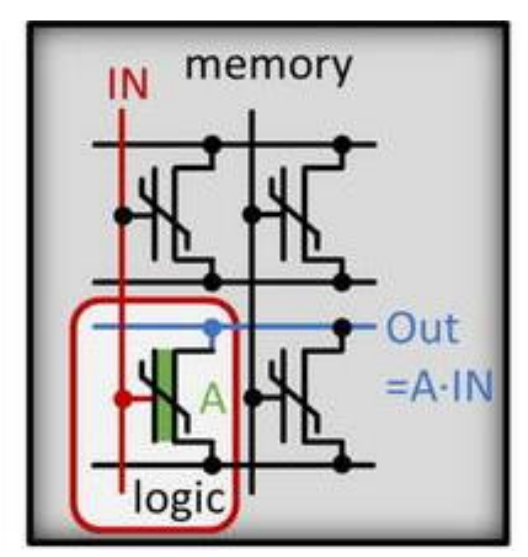
- Introduction
- Ferroelectric Materials for Semiconductor Devices
- Basic Ferroelectric Memory Devices
- **Ferroelectric enhanced Devices for Beyond von-Neumann Computing**
- Ferroelectric Devices for other Applications
- Summary and Conclusion

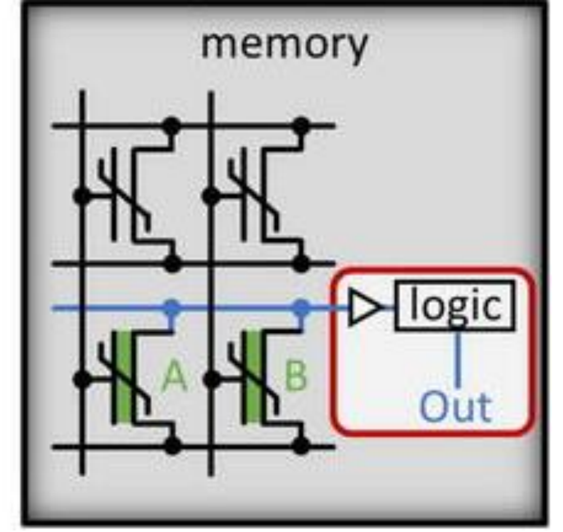
Ferroelectric devices beyond memories – Basic IMC and NVL blocks

FeFET

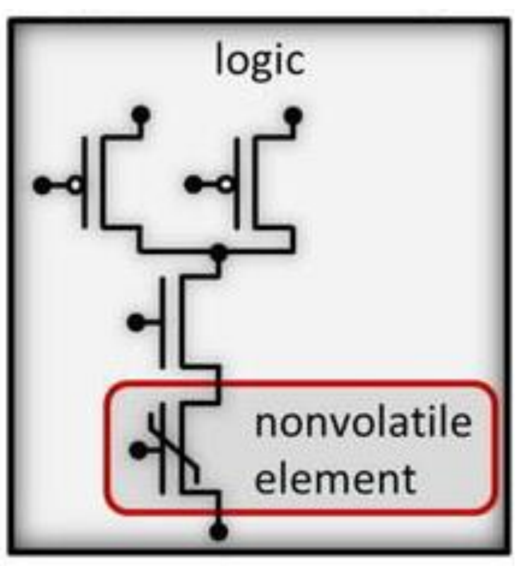


In-Memory Computing





Nonvolatile Logic

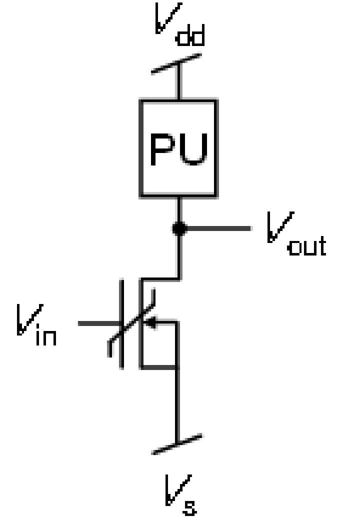


E. Breyer et al., APL 2021

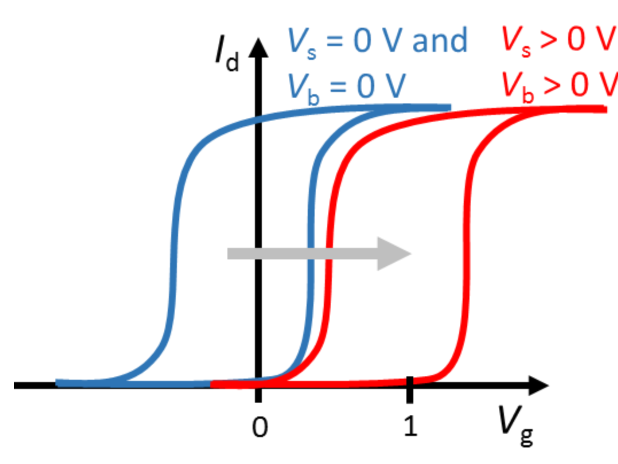
- Low current is the biggest issue in FTJ devices
- Hafnium Oxide with a thickness below 8nm is hard to stabilize in the orthorhombic phase
- Thinning after the crystallization can be an alternative

Ferroelectric devices beyond memories – Basic IMC and NVL blocks

Reconfigurable NAND/NOR gate



Principle of reconfigurable NAND/NOR gate



Truth tables for NAND and NOR gate

In	FE	Out (I)	Out (V)
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

In	FE	Out (I)	Out (V)
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

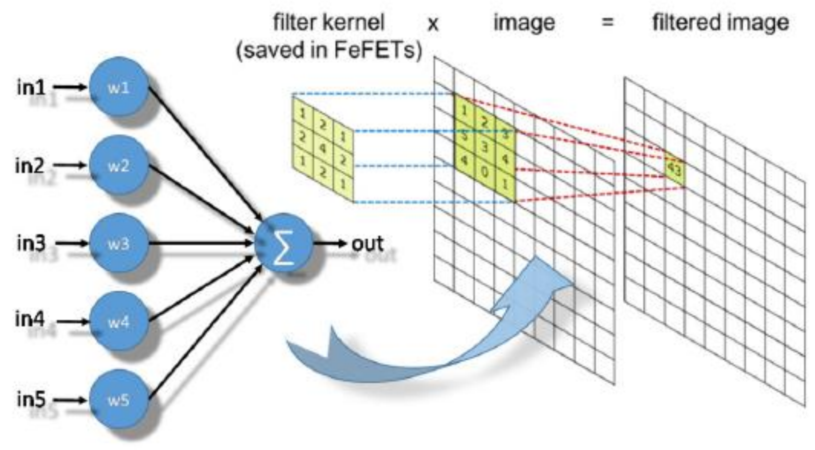
E. Breyer et al., IEDM 2017

E. Breyer et al., ISCAS 2018

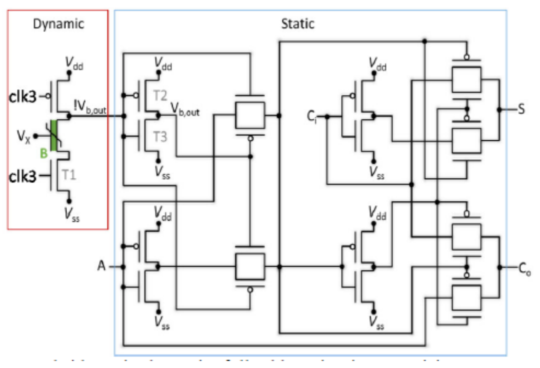
- One input is stored in form of the ferroelectric polarization
- The second input is applied to the gate
- Reconfiguration can be done by the source voltage or by the back gate voltage in the case of FDSOI

Ferroelectric devices beyond memories – Image Filter

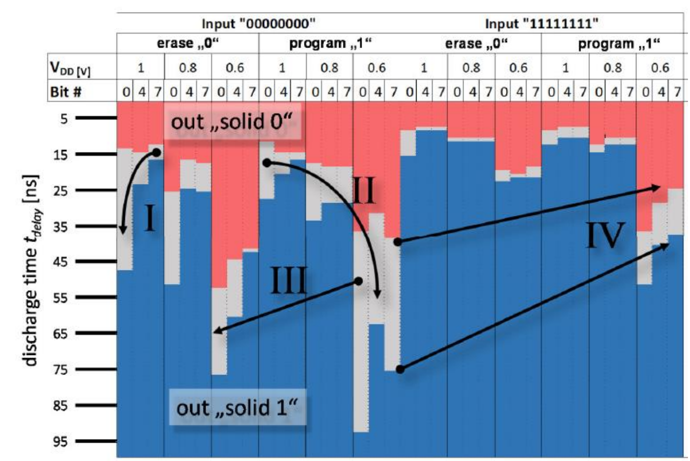
Single layer perceptron as image filter. Kernel coefficients are stored in FeFETs integrated into CMOS multipliers

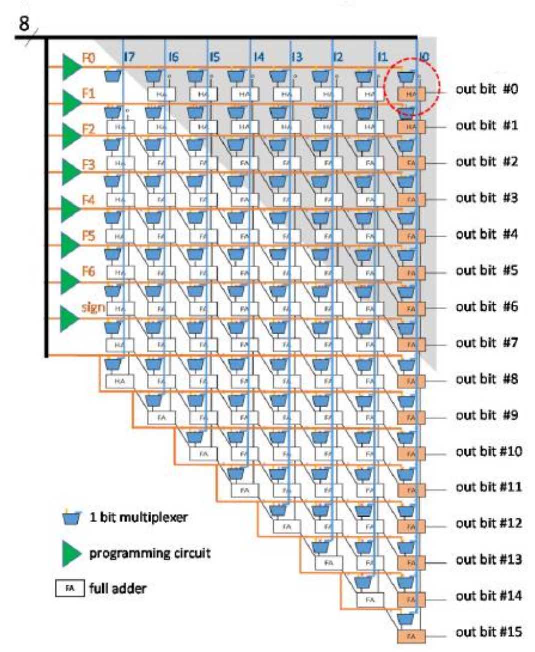


Hybrid static-dynamic full-adder (a) Schematic block diagram of the 8 bit multiplier consisting of 100 full-adders (b)



First result of image filter using solid patterns



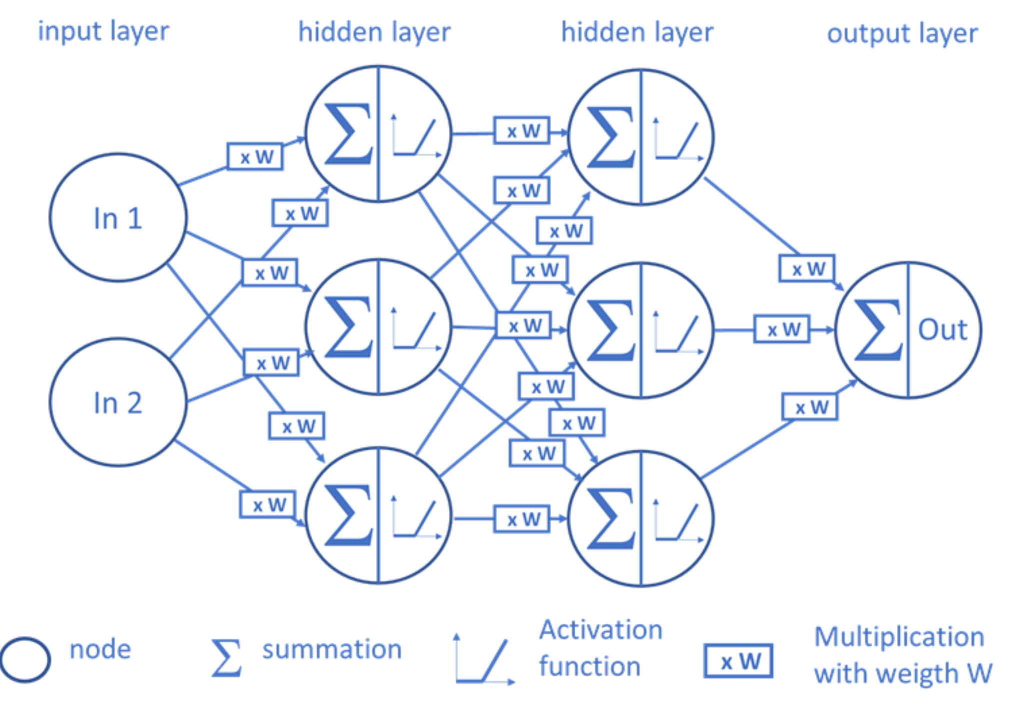


S. Sesazeck et al., unpublished results

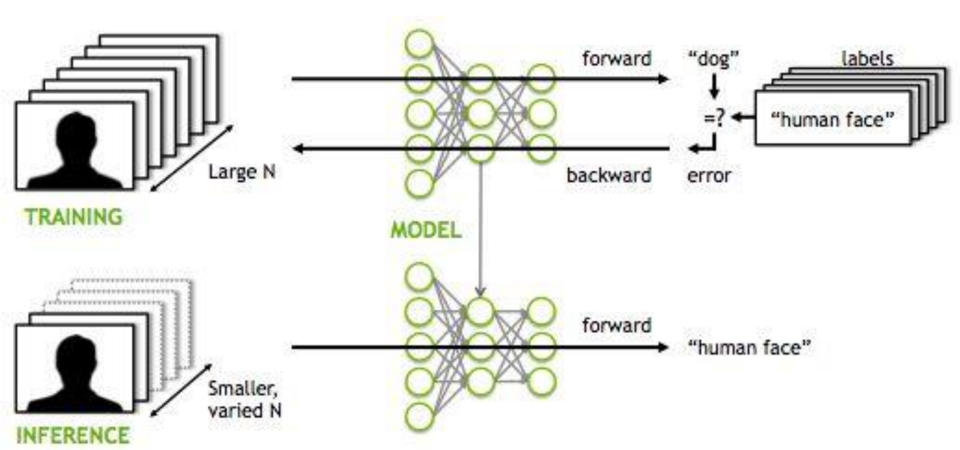
■ Integrating FeFET into adder/multiplier structures allows to keep the coefficients directly in the location they are needed

Ferroelectric devices beyond memories – Artificial neural networks

Schematic of an Artificial Neural Network



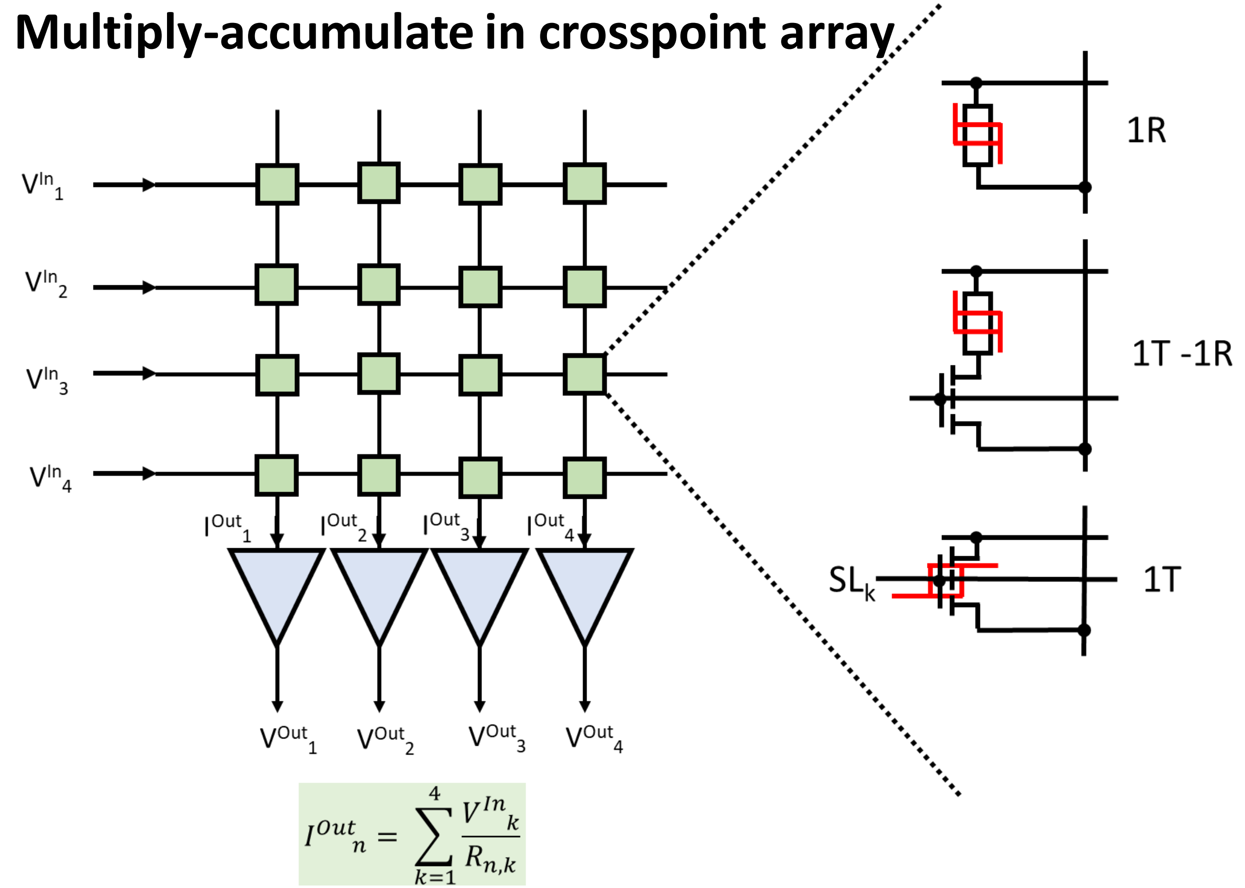
Training and Inference



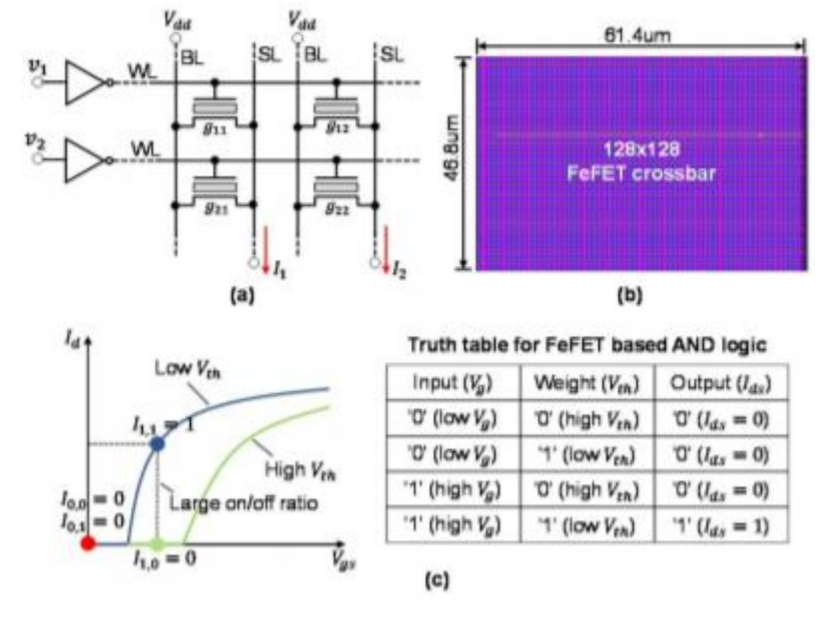
- A very simplistic model of the brain
- Nodes are connected via weights
- Inputs to nodes are summed and transferred to the output via an activation function
- Network needs to be trained using large amount of sample data
- Vector-Matrix Multiplication (VMM) is an essential operation both in forward and backpropagation
- Analog in Memory computing to realize VMM is an interesting option

Ferroelectric devices beyond memories – Artificial neural networks

Multiply-accumulate in crosspoint array



Vector Matrix Multiplication using FeFET



Input (V_g)	Weight (V_{th})	Output (I_{ds})
'0' (low V_g)	'0' (high V_{th})	'0' ($I_{ds}=0$)
'0' (low V_g)	'1' (low V_{th})	'0' ($I_{ds}=0$)
'1' (high V_g)	'0' (high V_{th})	'0' ($I_{ds}=0$)
'1' (high V_g)	'1' (low V_{th})	'1' ($I_{ds}=1$)

Y. Long et al., ICCAD, 2018

- Vector-Matrix multiplication (VMM) is a basic operation in ANN
- In a cross-point array VMM can be realized using Ohm´s Law (Multiply) and Kirchhoff´s Law (Accumulate)
- Either FTJs or FeFETs can be used to store the weights
- Details in FET based architectures can be different (e.g. separate SL or 2T)

Ferroelectric devices beyond memories – spiking neural networks

IEEE ISAF 2023

possible circuit/device implementations of neuro-biological processes

Axon
Soma
Dendrite
Synapse

Summation of weighted spikes → matrix-vector multiplication in crosspoint arrays
V_1 V_2 V_3

→ FeFETs or FTJs with analogue switching

Integrate and fire neuron → pulse accumulation in RRAM and PCM
input, Time, V_m, Time

→ Accumulative switching in scaled FeFETS

Long-term synaptic plasticity → set/reset transitions in non-volatile RRAM and PCM
ΔG, Δt

← FeFETs or FTJs with low depolarization field

Short-term synaptic excitation → set transition in volatile RRAM
input, Time, output, Time

→ FeFETs or FTJs with large depolarization field

D. Ielmini et al., APL Materials 2020

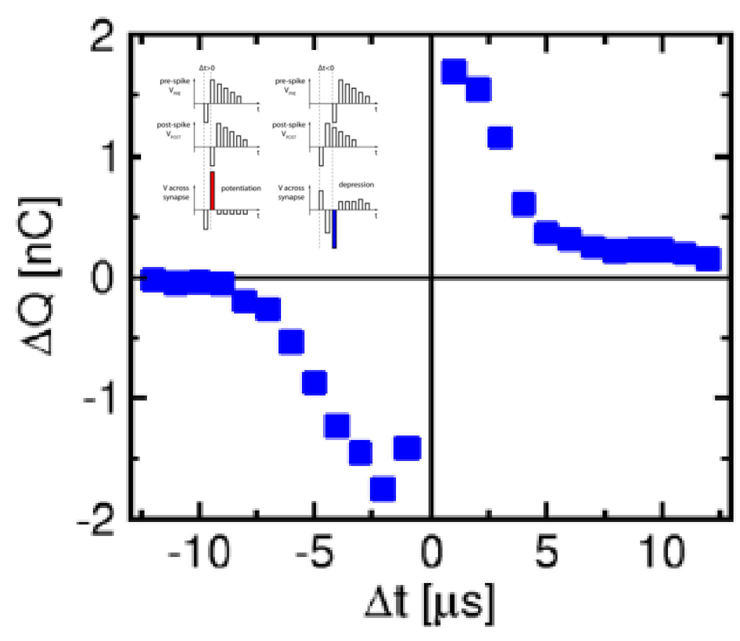
- Important neuro-biological processes can be mimicked by modified memory devices
- The rich implementation variety of ferroelectric devices gives many possibilities
- STDP –like behavior is obtained in FeFET and FTJ
- The accumulative switching in scaled FeFETs can be used to mimic the integration and fire behavior of a neuron

Ferroelectric devices beyond memories – Synapses

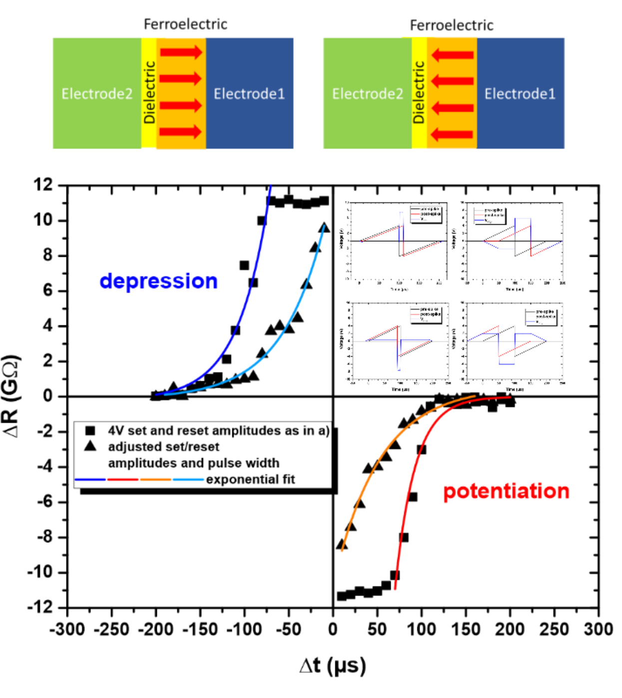
FeFET operated as synapse

pre-spike
R
pre-neuron
post-neuron
post-spike

STDP like behavior in FeFET



STDP like behavior in FTJ

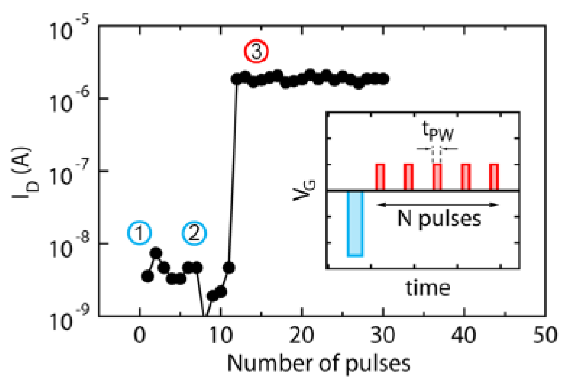


- In a multi domain device the channel current can be controlled either by the voltage or the time of the programming pulses
- Using an additional resistor a two terminal synapse can be mimicked
- STDP –like behavior is obtained
- The three terminal device can also be used directly to decouple prog. and read

H. Mulaosmanovic et al., VLSI 2017

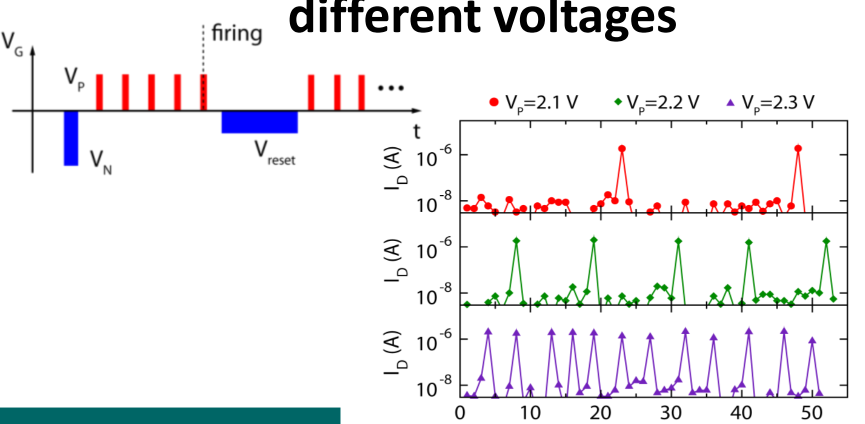
Ferroelectric devices beyond memories – Neurons

Accumulative switching of scaled FeFET



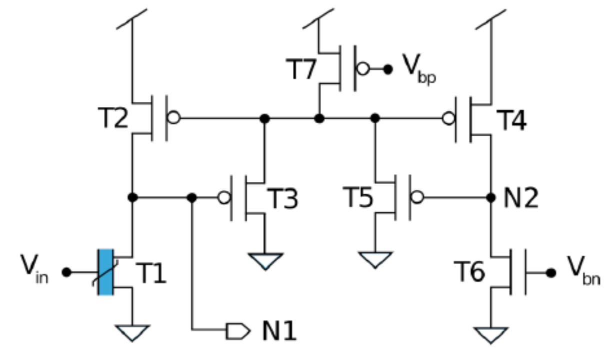
H. Mulaosmanovic et al., ACS AMI 2018

Repeated integrate and Fire cycles for different voltages



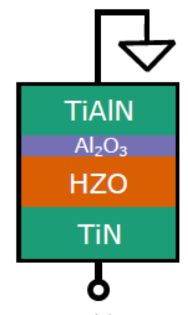
H. Mulaosmanovic et al., Nanoscale 2018

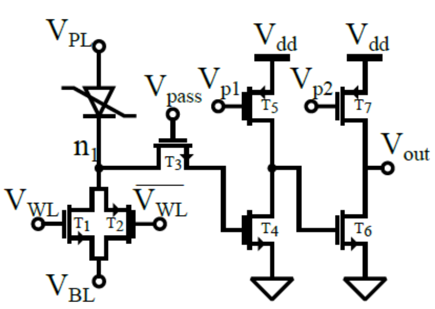
7T Neuron circuit



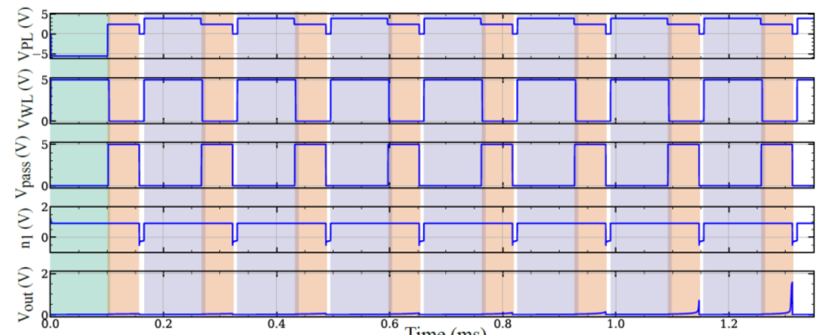
B. Suresh et al., ICECS 2019

FTJ based integrate and fire neuron





Simulation of FTJ based integrate and fire neuron up to the first pulse



P. Gibertini et al., ICECS 2022

- Ultra-scaled FeFETs exhibit accumulative switching
- The effect can be used for mimicking biological neurons
- current FTJ can be used in gain cell configuration

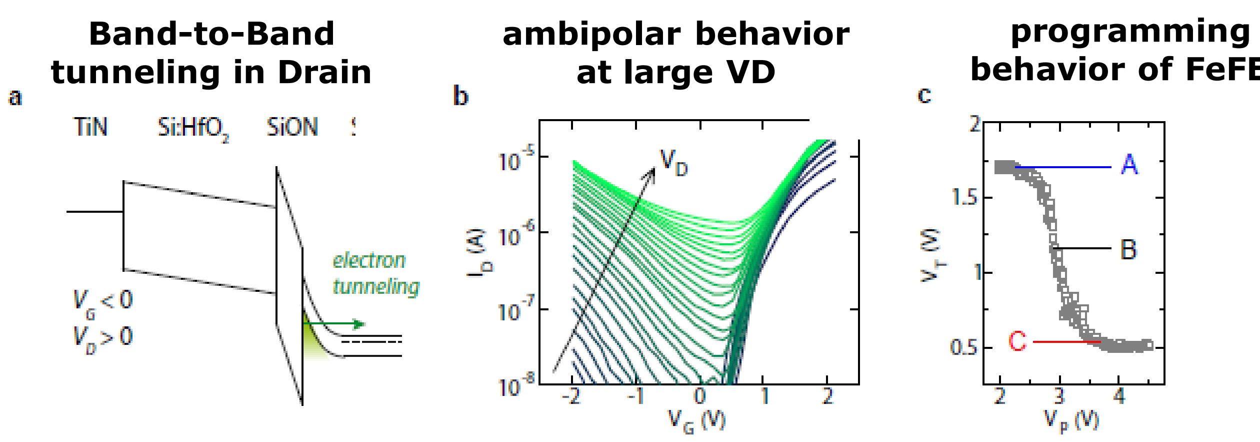
Outline

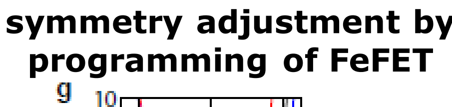
- Introduction
- Ferroelectric Materials for Semiconductor Devices
- Basic Ferroelectric Memory Devices
- Ferroelectric enhanced Devices for Beyond von-Neumann Computing
- Ferroelectric Devices for other Applications
- Summary and Conclusion

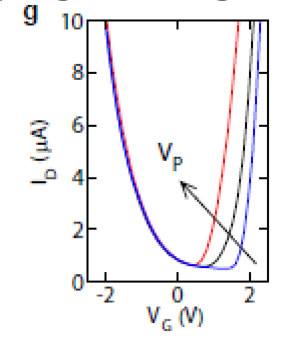
Ferroelectric FETs for frequency multiplication and mixing

Frequency doubling and mixing: Principle of tuning ambipolarity in a FeFET device

Band-to-Band tunneling in Drain | ambipolar behavior at large VD | programming behavior of FeFET | symmetry adjustment by programming of FeFET

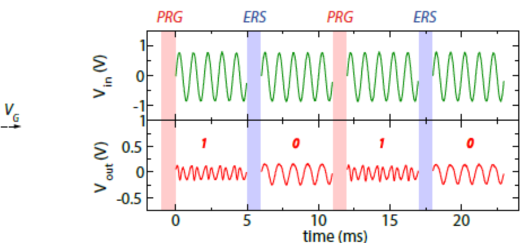




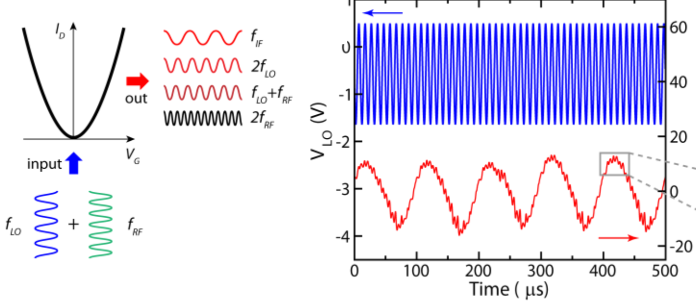


Principle of frequency doubling using FeFET

Programmable frequency doubling



Demonstration of frequency mixing



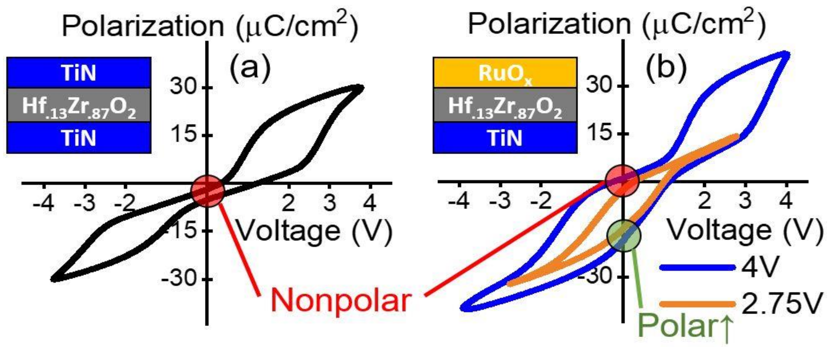
H. Mulaosmanovic et al., Nature Electronics 2020

H. Mulaosmanovic et al., ACS AMI 2020

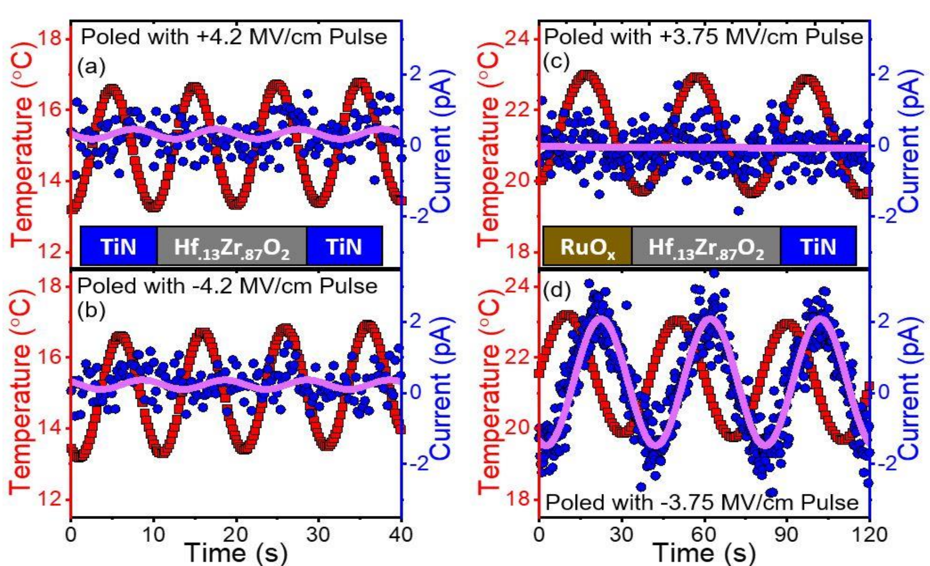
- GIDL can be influenced by programming and erasing in a FeFET
- In an extreme case an ambipolar characteristic can be achieved
- Frequency doubling can be turned on and off by programming/erasing the FeFET

Switchable Pyroelectricity

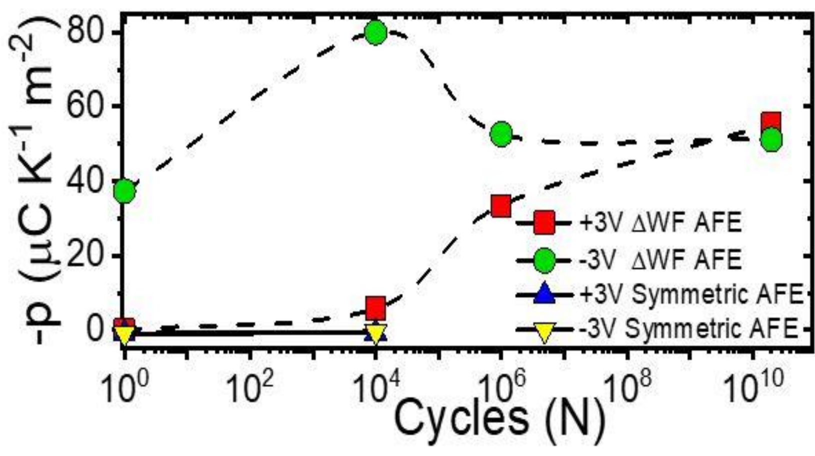
Antiferroelectric Hysteresis without (a) and with (b) internal bias field



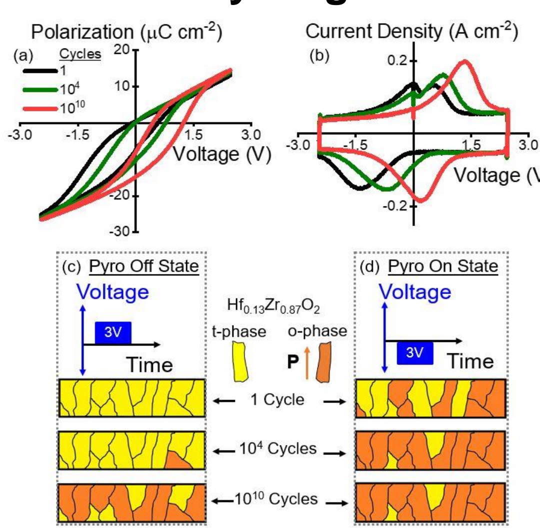
Antiferroelectric Hysteresis without (left) and with (right) internal bias field after poling



Pyroelectric coefficient of symmetric and unsymmetric samples



Field cycling model

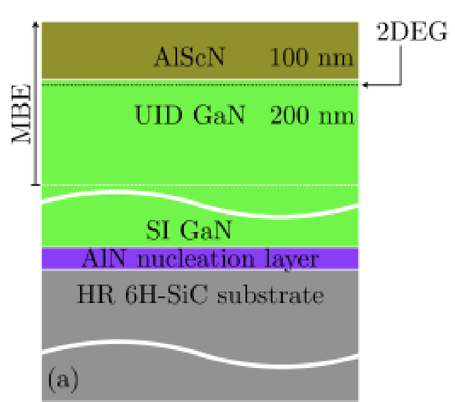


- Antiferroelectric hysteresis can be shifted to show a window at 0V
- He shifted hysteresis can be switched between a polar and a non-polar state
- Pyroelectric response can be switches on and off accordingly

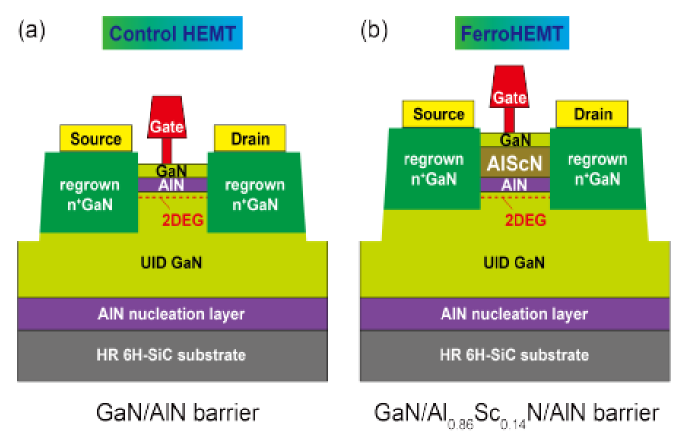
P.D. Lomenzo et al., Transducerss 2023

Ferroelectric HEMT using AlScN

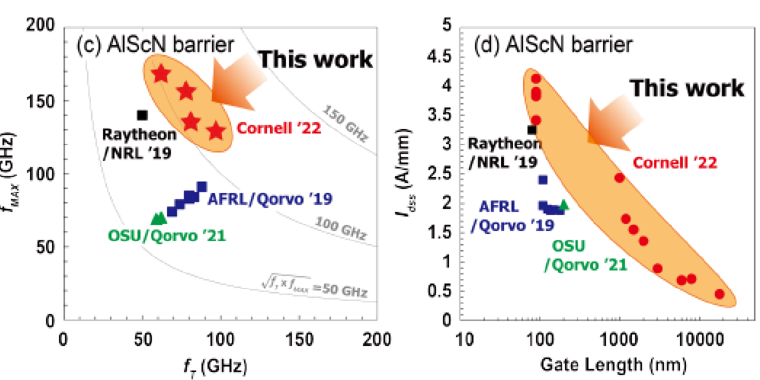
Epitaxial AlScN/GaN heterostructure



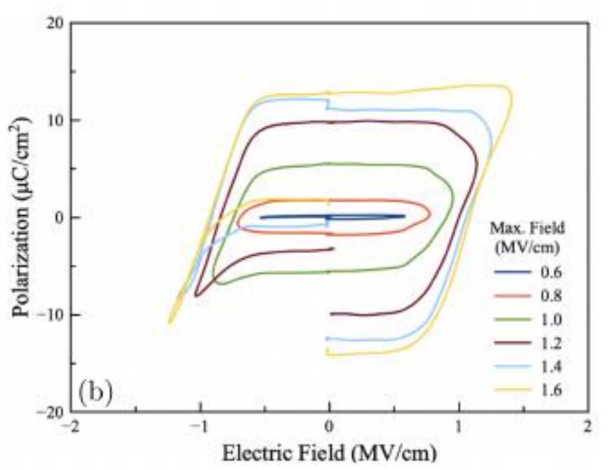
Std. HEMT (a) and Ferro HEMT (b)



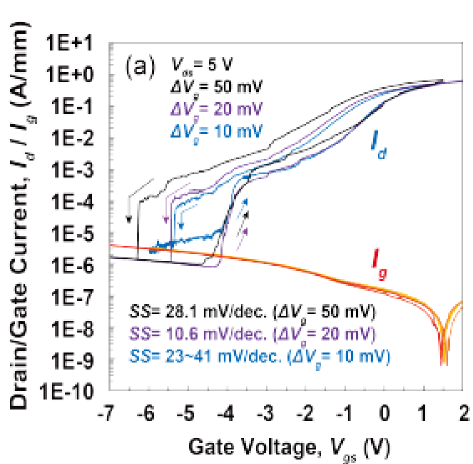
Benchmarking

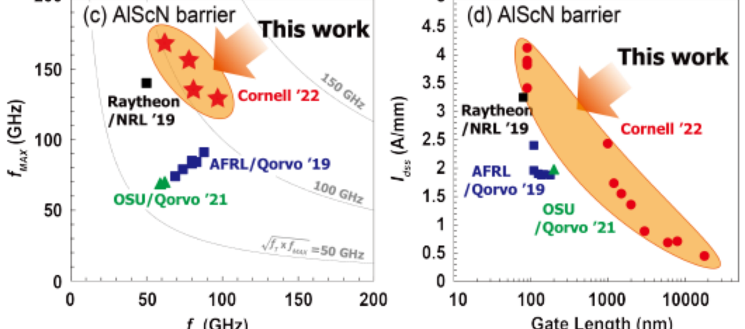


Hysteresis of epitaxial AlScN/GaN heterostructure



Ferro HEMT transfer curves



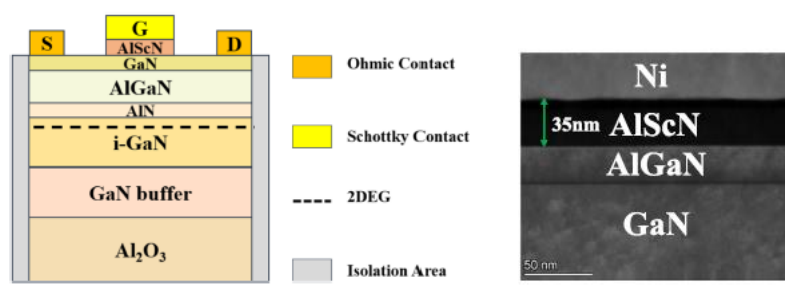


- AlSCN is an Ideal FIT to GaN HEMT Technology
- Ferroelectric layers allows to tune the threshold voltage by voltage pulses
- In this example the AlScN takes the role of the AlGaN in creating the 2DEG

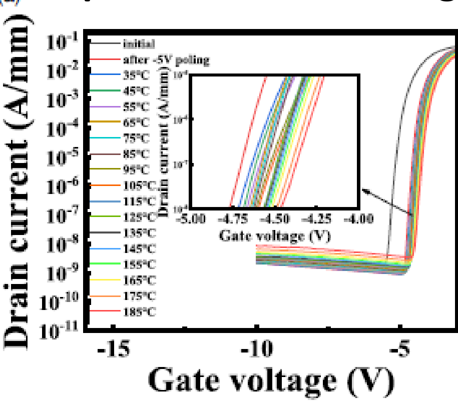
J. Casamento et al., IEDM 2022

Ferroelectric HEMT using AlScN

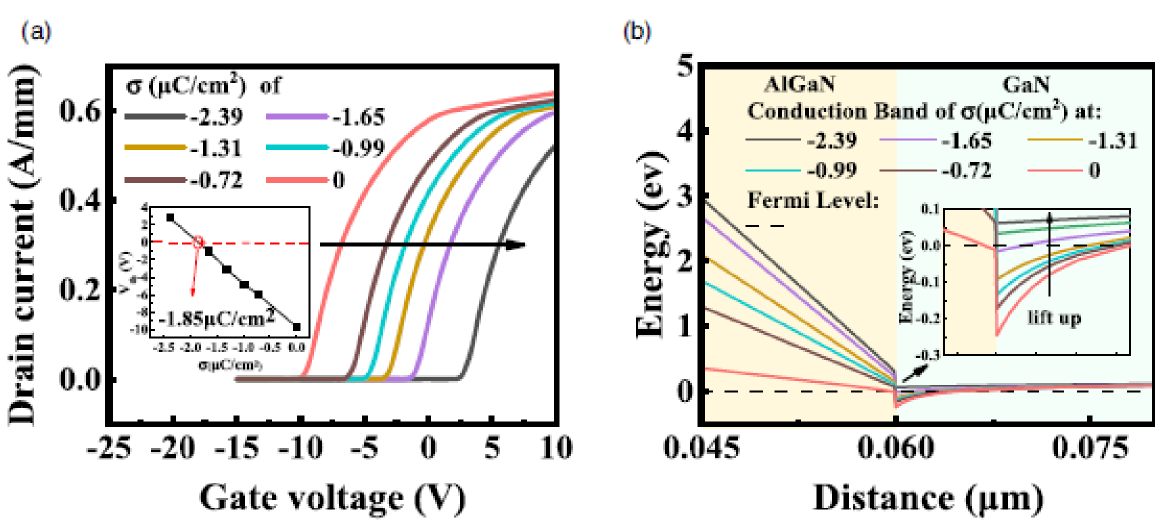
AlScN/GaN/AlGaN/AlN/GaN HEMT



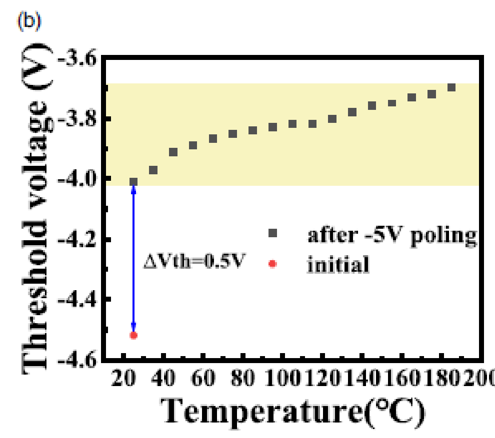
Experimental VT tuning



Simulated tranfer curve (a) and band diagram (b)



Temperature dependence of programmed VT

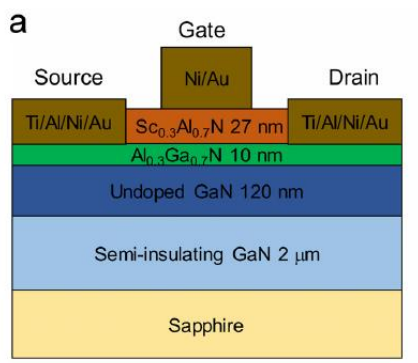


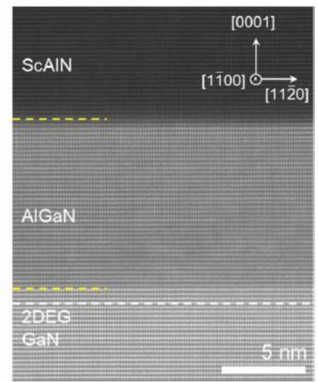
- Here AlScN is used as a ferroelectric insulator in a MISHEMTstructure
- Nice VT window in simulation, but much lower one observed experimentally

Z. Zhao et al., Apl. Phys Exp. 2023

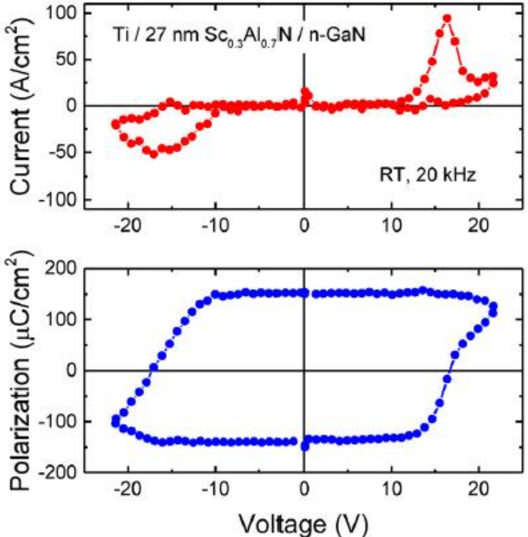
Ferroelectric HEMT using AlScN

MBE grown AlScN/AlGaN/GaN HEMT

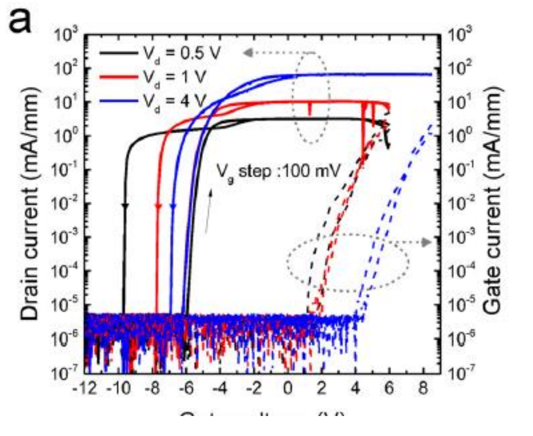


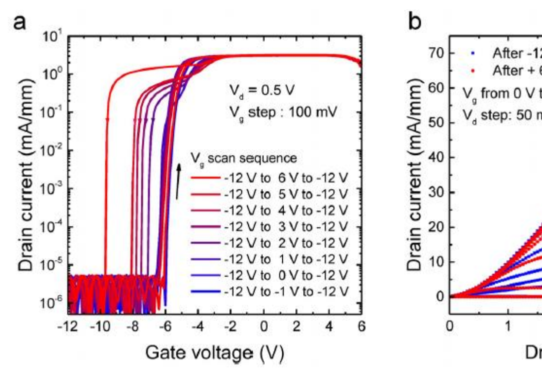


Hysteresis of MBE AlScN MIM capacitor

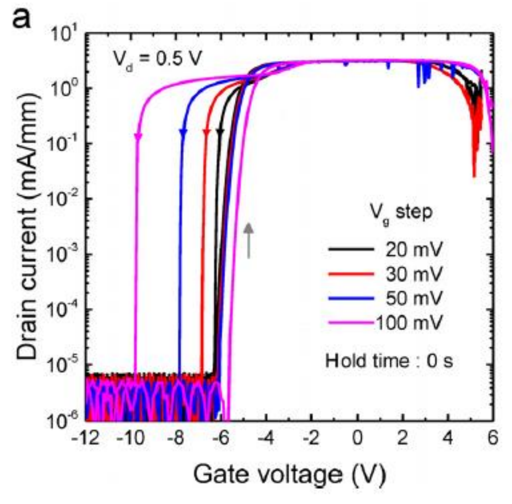


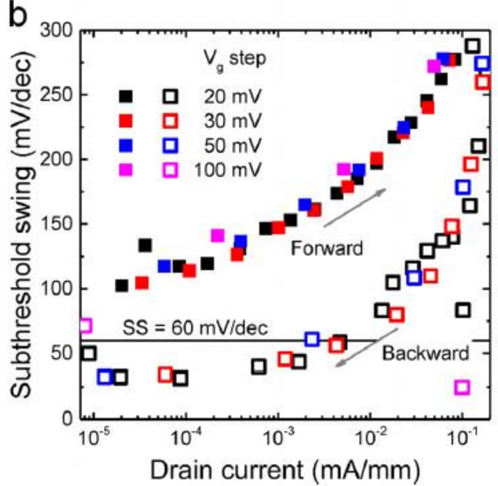
Std. HEMT Ferro HEMT and Ferro HEMT





Ferro HEMT transfer curves



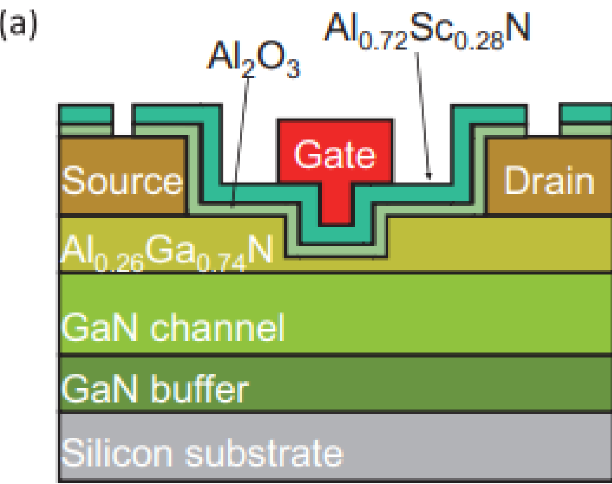


D. Wang et al., Apl. Phys Lett. 2023

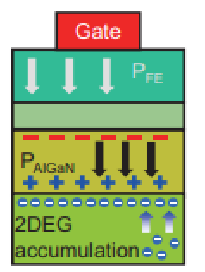
- Again the AlScN is used in a MISHET structure
- Reasonable VT window

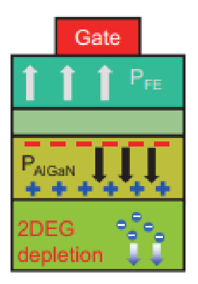
Ferroelectric HEMT using AlScN

AlScN/Al2O3/ AlGaN/GaN HEMT using sputtered AlScN

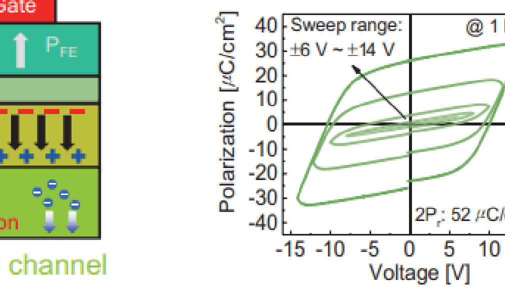


(sputtered AlScN)/Al2O3/ AlGaN/GaN gate stack and P-V loops of MIM cap

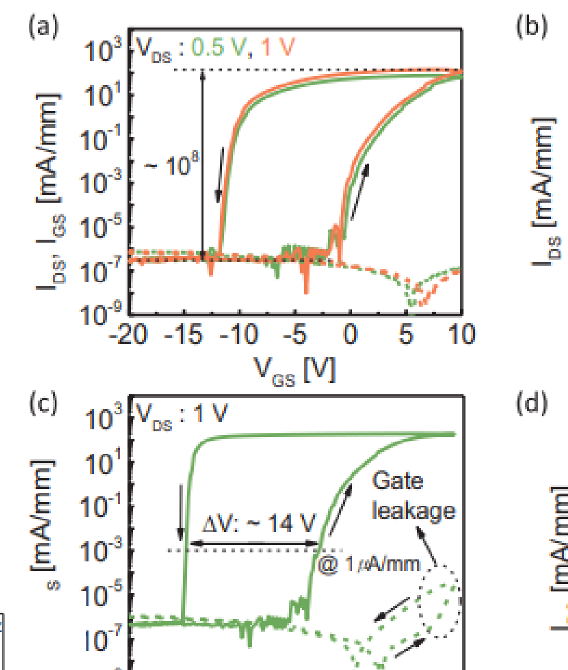


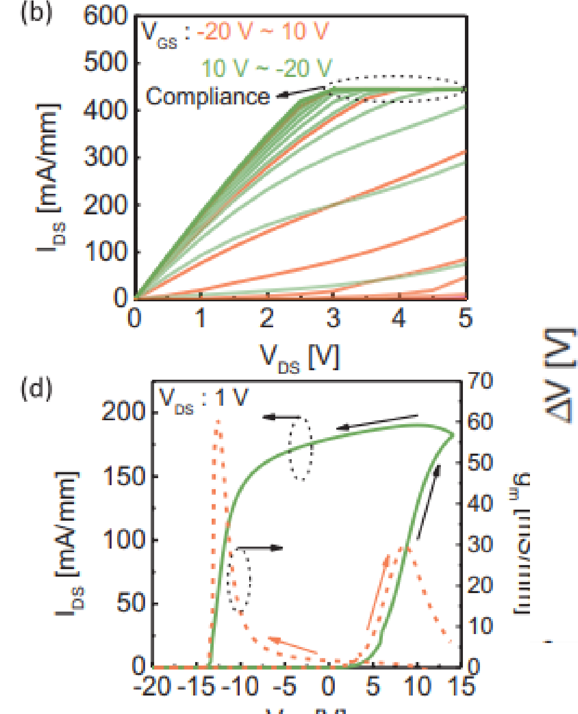


AlScN/Al_2O_3/AlGaN/GaN channel

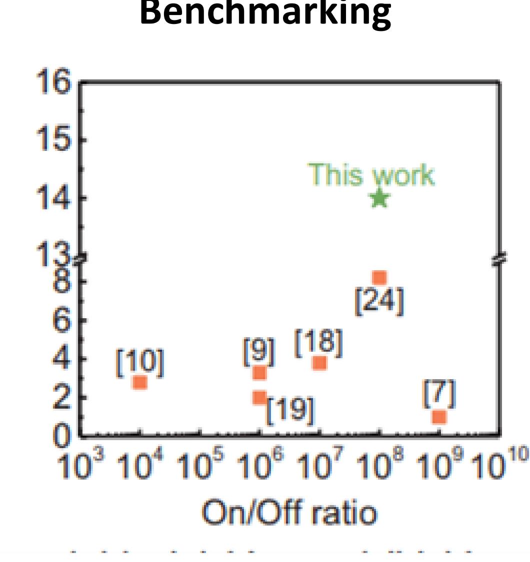


Electrical characterization of (sputtered AlScN)/Al2O3/ AlGaN/GaN HEMT





Benchmarking

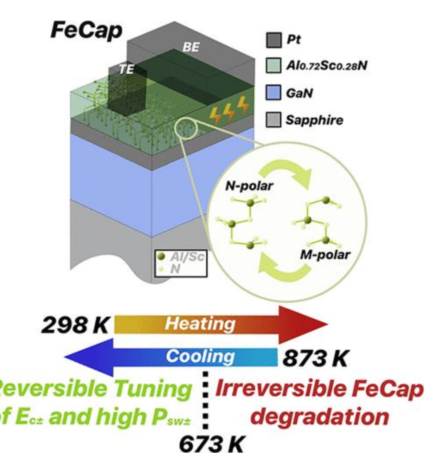


J. Y- Yang et al., IEEE EDL 2023

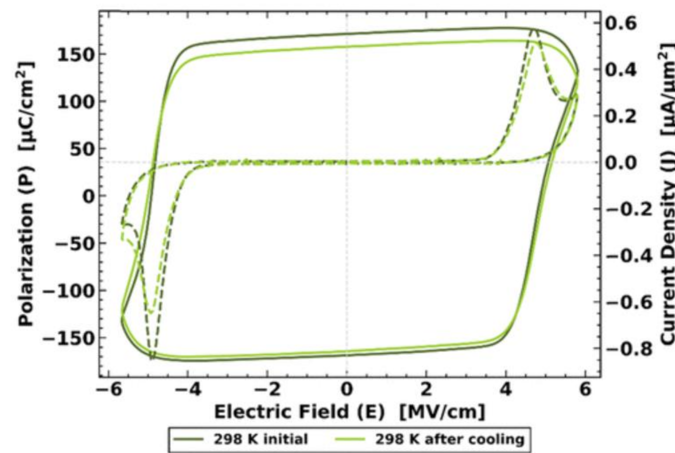
- By using a recessed channel a VT window above 10V is achieved
- Device can be switched between Depletion (D) and Enhancement (E) mode

Temperature stability of ferroelectric AlScN

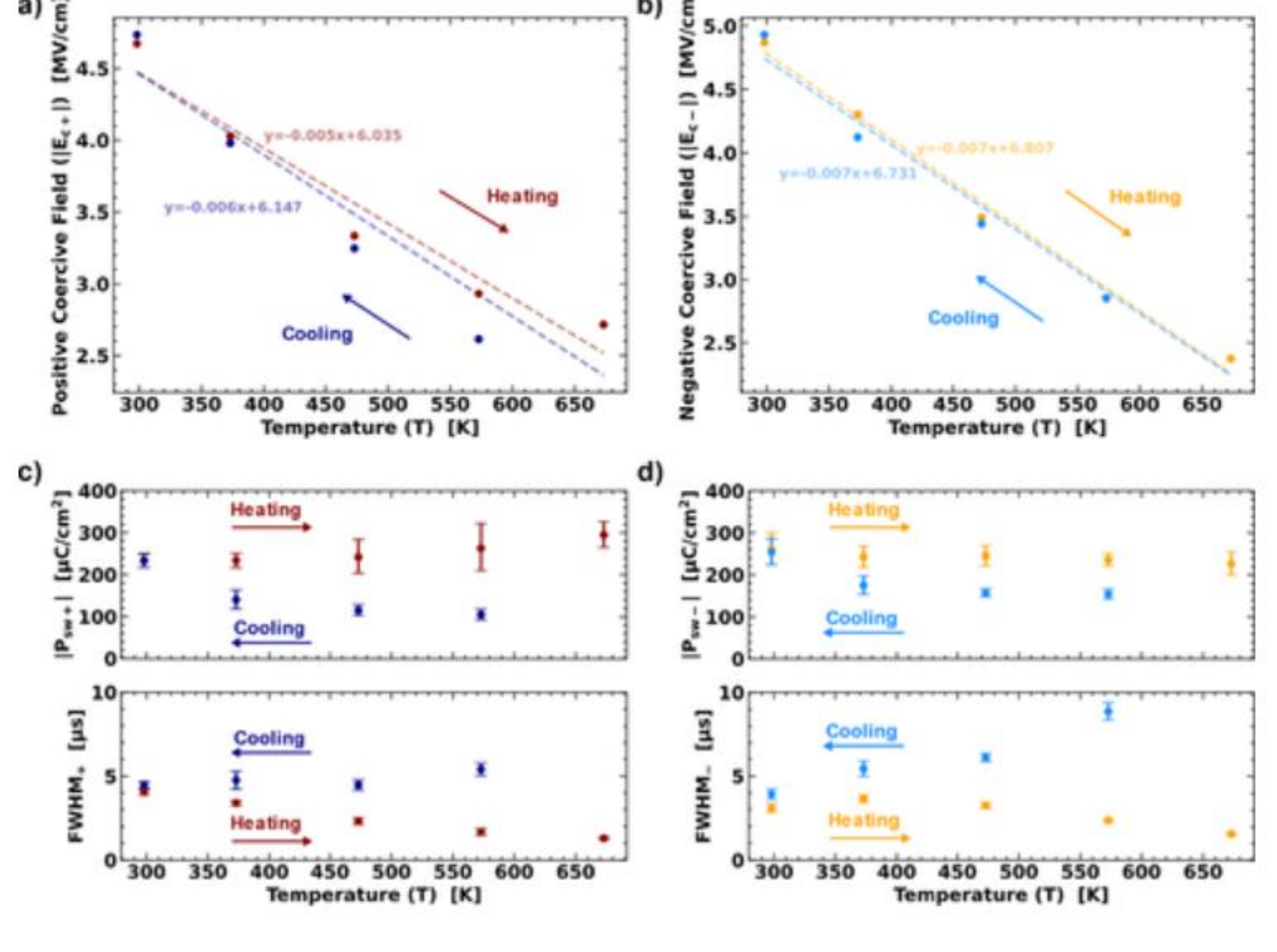
Investigated structure



Hysteresis bevor and after temp cycle to 673K



Coercive field and polarization as a function of temperature up to 673K

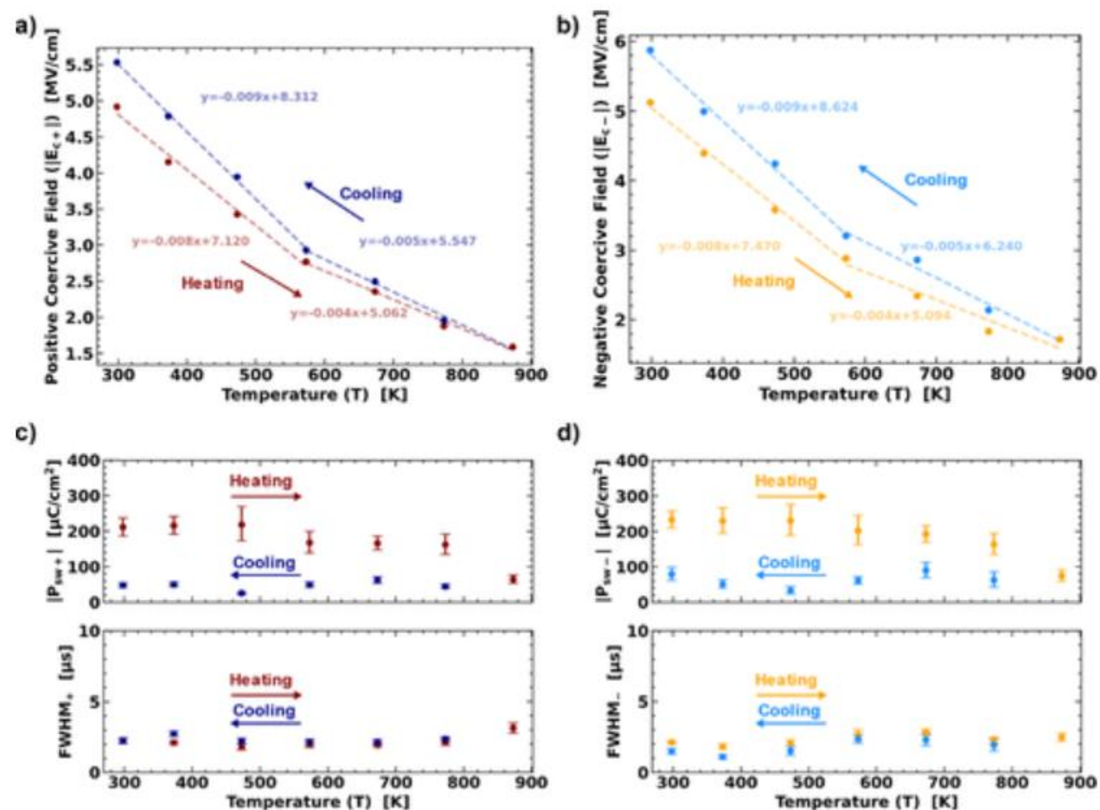


R. Guido et al., Appl. Mat. & Int. (2023)

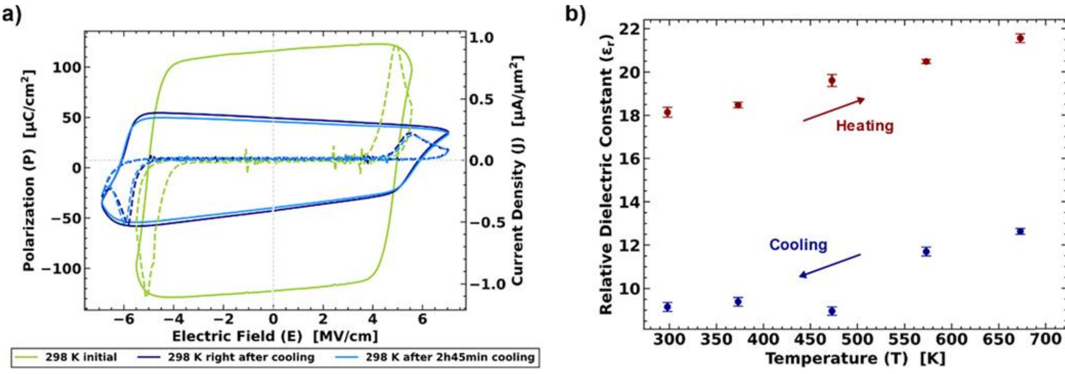
- Up to 673K AlScN shows high stability
- Useful for high temp and power electronics applications

Temperature stability of ferroelectric AlScN

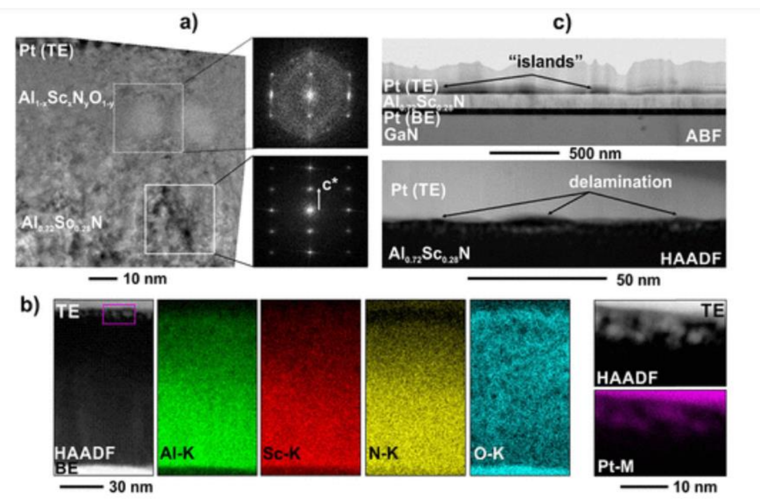
Coercive field and polarization as a function of temperature up to 873K



Hysteresis bevor and after temp cycle to 873K as well as temp dependent permitivity



Structural analysis after heating up to 873K



- After heating to 873K AlScN shows irreversible degradation
- There seems to be a transition point at almost 600K

R. Guido et al., Appl. Mat. & Int. (2023)

cfaed

Summary and Conclusion

- Ferroelectric devices are very energy efficient in the programming operation
- Ferroelectric hafnium oxide can overcome the integration issues observed with perovskite based ferroelectrics for CMOS while AlScN seems to be an ideal fit for GAN HEMTS
- Three different read operations lead to there different memory cell concepts
- Array level demonstrators fabricated in industry compatible CMOS lines are available both for FeRAM and FeFET based on hafnium oxide
- In-Memory computing and nonvolatile logic can be realized by taking advantage of the fact that FeFETs can be integrated close to regular CMOS transistors and can be programmed and erased using moderate voltages.
- FTJ and FeFETs can be used to realize artificial synapses and FeFETs enable the accumulation required for artificial neurons to realize spiking neural networks
- Many more applications that use either the ferroelectricity ort the associated piezo- and pyroelectricity can now be integrated on a chip

Thank You

Thanks to all current and former team members of the ferro team at NaMLab!

- ☐ Thanks to all cooperation partners from Fraunhofer IPMS, FMC, Leti, NC State University, RWTH Aachen, Kiel University Tokyo Institute of Technology, Seoul National University, ….

- ☐ Thanks to GLOBALFOUNDRIES for providing their 28nm and 22nm FerroFET technology and Sony as well as Leti for their FeRAM testchips
- ☐ Thanks to you for your attention

“Parts of this work was financially supported by the European Fund for Regional Development EFRD, Europe supports Saxony, and by funds released by the delegates of the Saxon State Parliament as well as by DFG ”

Dieses Maßnahme wird mitfinanziert durch Steuermittel auf Grundlage des von den Abgeordneten des Sächsischen Landtages beschlossenen Haushaltes.