

Virtual Platforms to Shift-Left Software Development and System Verification

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cadence









Shift-Left: the Solution We All Talk About







Shift-Left: the Solution We All Talk About







Hybrid: A Critical Part of the Puzzle







2022 DVCON

Hybrid: A Critical Part of the Puzzle







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SW

System

Where is Hybrid Applicable?



What About the Cyclic Dependency?







Successively Refined Abstract Platforms









Successively Refined Abstract Platforms









Successively Refined Abstract Platforms









Extend Accuracy with Hybrid Platforms

Driver 2

OS

Driver 1

CPU





Emulation and Prototyping



- Extend with Emulation and FPGA Prototyping to run with the most accurate representation of the design ASAP using platforms running 100's of MHz
- Typical Use-cases
 - Bring-up and test Linux and drivers
 - Bring-up and test Android
 - Targeted benchmarks and performance optimization
 - Critical application bring-up





Example Hybrid System

Execute SW at 100MHz With standard or custom processor models

Plug and Play Integration with RTL SoC-specific transactors and RTL I/F

Validate SoC + OS at 5-10 MHz High-performance memory coherency

Reduce SoC Debug Effort System Messages HW / SW Debuggers







Typical Hybrid Platform Creation and Software Bring-up Flow

- Create New Hybrid Platform
 - Start with Example hybrid platform
 - Save-As flow for new hybrid platform
 - Add/Remove virtual models (as needed)
 - Configure parameters and bind ports
 - Rewire interrupt and memory map
 - Add/Remove RTL stubs (as needed)
 - Configure Hybrid Adaptors for connecting to new RTL design
- RTL changes to connect Helium Hybrid Adaptors
 - CPU Architecture Example
 - CPU RTL wrapper details and configuration options
 - GIC wrapper (GIC600)
 - Smart Memory (LPDDR5)
- Build & Run Linux on Hybrid Platform and enable SW debug





Getting started with Example: A510 Hybrid Platform

Save to Catalog

Choose Starter Platform

🖁 Catalog Browser 🕱 🏠 Project Explorer 🗧 🗖	
🕀 🛋 🐴 🖬 😽 i 🔻	Helium Model Catalog
type filter text 🛛	
 Helium Model Catalog Cadence_com Cadence_com<	 Pre-populated in GUI Provides several Base Models Several Reference Platforms examples shipped Get a jumpstart and quickly build complex design Alter Memory Map, add/remove Peripheral as needed
▶ e a510_gic600_virtio ▶ c a510_gic600_virtio	
♦ @ a510_gic800_virtio_axi_nybrid ♦ @ a710_gic700_virtio	
▶	
🕶 🌐 util	

Add / Remove Virtual Models arameter Config / Port Binding Rewire Interrupt and Memory Map





Debu

Add/Remove virtual models (1/2)



Save to

hoose Starter Platform

dd / Remove Virtual Models

/ Port Binding

Rewire Interrupt and Memory Map



Add/Remove virtual models (2/2)

Copy and paste with connections also creates new instances

Save to

hoose Starter Platforn

d / Remove

/ Port Bindin

- When you want to save work by re-using groups of connected instances from other platforms, simply copy a group of connected instances and paste them into your platform
- No need to <u>redo connections between components</u> and <u>set parameter values</u> – they get copied with the group
- Make sure to make any **required port connections** from ports in the group to **external instances**

Select the uart, term, tty_mon instances in the design editor, right-click and choose Copy or use <Ctrl-C>

To create a new instance of the selected components, choose a platform in an open editor, select the appropriate scope, right-click and choose Paste or use <Ctrl-V>

Design Editor			
type filter text			
Name	Туре		Valu
👂 🖻 keyboard	pl050_km		
A ethernet	smc91c111_eth	ernet	
👂 🖪 bremse	sim_throttle		
Image: Slirp_wrapper	slirp_wrapper	Copy	Ctrl+C
👂 👜 sysctl	sp810_sysctl	Paste	Ctrl+V
🕨 🔤 mmc	pl181_mmci	X Delete	Delete
👂 🖪 sdcard	sdcard		10.0100
pvbus_m_64_32	simple_buswidt	Add to Memory Map	
▷ Imagic_pvbus_s_32_64	simple_buswidt	🍄 Go to Catalog Model	
Image: Simple_converter	simple_convert	Revert to Catalog Definition	
Image: A state of the state	simple_memor	🈂 Change Instance Type	
ddr_ram0	simple_memor	🏷 Update Interface	
Simctrl	simctrl	📑 Add Hierarchy	
٥ ق uart	pl011_uart	E Add Port	
🕨 🖪 dualtimer	sp804	Add Signal	
ک بھ term	term	🔆 Add Stub	
🕨 🖪 tty_mon	ttymonitor	Add Field	

Hybrid Adaptors & RTL Connectior

Rewire Interrupt and Memory Map Add / Remove RTL Stubs



Debug

Parameters Configuration • Visualize platform ins their values	S tance param	Choose Starter Platform	Save to Catalog	Add / Remo Virtual Mod	Parameter Config / Port Binding Use U recon chang mode	Rewire Interrupt and Memory Map Add / Remove RTL Stubs pdate Interface to figure instance when you re parameters that affect I interface	Hybrid Adaptors & RTL Connection RTL Side changes Build & Run Debu Go to Catalog Model Update Interface Change Instance Type Revert to Catalog Definition
Design Editor							E 🖄 🕀 🕞 💷 📭 💵
type filter text	Platform Assembl	y Design Editor					0
 ARM_Fast_Models_Global_Para Parameters (12) Im_global_quantum scx_set_min_sync_latence quantum_seconds scx_start_cadi_server_state scx_start_cadi_server_runt scx_start_cadi_server_de scx_load_application_all scx_print_statistics scx_parse_and_configure tarmac_trace 	y y burt bug Global paramu ARM Fast Mor	Type ARMPlatform double double double bool bool std::string std::string bool eters common to all del instances	Value 0.00010 0.0001 false false false true alse	00 View and e	Details The system glob The minimum sy The system glob Set to true to sta Set to true to ena Set to true to ena The application t The file of the plu Set to true to log Parses command dit individual mod	al simulation quantum time nchronization latency. Measu al simulation quantum time rt a CADI server the simulation immediately able debugging through a plu o load ug-in to load able printing of simulation st CADI calls I-line options and configures lel Fast Models Tarmac Trac	in seconds. Set either this or quantum_seconds param ured in seconds in seconds. Set either this or tlm_global_quantum par r after CADI server has been started ig-in atistics the simulation accordingly e
 A sram Ports (2) Parameters (10) verbosity size enable dmi 		simple_mem std::string unsigned long bool	ory<32> g long	0x2000000	Per-instan Set size of	ce verbosity, always overrides gl simple memory in bytes. Range to enable DMI. Range: {true* fai	lobal verbosity. Range: {0,100,200,300,400,500} or {SC_NON :: {0x1,,0x100000*,0x100001,,2^63}

SYSTEMS INITIATIVE

Handling Port Bindings

Method1: Bind Selected Port

- Port binding through 'Ports' tab.
- Select the unbound port in LHS, then the ports eligible to be bound will be shown in RHS. Select the port and right click and do "Bind Selected Port"



Save to Catalog

Choose Starter Platform

Add / Remi

Ports Select the ports from the unbound list to view its candidate ports and create the bindings Unbound **Bind Candidates** E spi_in_5 -03 uart*intr Name Name Type **Remaining Binds** SC OUT 📧 uart 0.int •1" Bind Selected Ports K uart 1.intr SC OUT 1 ●L[®] Force Bind SC_OUT ■ uart 3.intr SC OUT 1 Auto Stub Selected Unbound Ports •13 Auto Stub selected ports with value •C Expose as Hierarchical Port In Go Home Go Back 🖒 Go Into Expand to see completed bindings Design Tree Ports

Rewire Interrupt and Memory Map

Config / Port Binding

Remove Hybrid Stubs & RTL C

Hybrid Adaptors & RTL Connection Debi

Slide 20

AW9	Should mention the Auto stub capability here;
	Andrew Wilmot, 11/15/2021

- AB7 Yes. I will add call out and talk about it. Ankit B, 11/16/2021
- AB23 Added call out Ankit B, 11/17/2021

Memory Maps In Helium Platform Assembly

Memory Man

- Create, View and Edit Memory Map using Memory Map View
- Memory Map creation is eased by automatic entry creation and automatic connections when using the Cadence router

type filter text				
Port	IIII Base Address	IIII End Address	Size 🗐 Offse	t 📲 Details
🛛 stub_sram	0×0400000	0x0403FFFF	0x00040000	Stub, DMI, AllocMem
🛛 stub_unknown	0x1C0E8000	0x1C0E8FFF	0x00001000	Stub, DMI, AllocMem
■ stub_usb	0×1B000000	0×1B000FFF	0x00001000	Stub, DMI, AllocMem
vexpress_v9.aci.bus	0x1C040000	0x1C04FFFF	0x00010000	Connected
vexpress_v9.bridge.tsocket				Default, Connected
vexpress_v9.dualtimer_0.bus	0×1C110000	0×1C110FFF	0×00001000	Connected
vexpress_v9.dualtimer_1.bus	0x1C120000	0×1C120FFF	0x00001000	Connected
vexpress_v9.dualtimer_2.bus	0x1C130000	0x1C130FFF	0x00001000	Connected
vexpress_v9.dummy_sram.tsocket	0x2E000000	0x2E1FFFFF	0x00200000	Connected
vexpress_v9.ethernet.tsocket	0×1A000000	0×1A0000FF	0x0000100	^_auto_simple_buswidth_converter_26.isocket
vexpress_v9.gic.pvbus_s	0x2C000000	0x2CFFFFFF	0x01000000	^_auto_simple_buswidth_converter_22.isocket
vexpress_v9.lcdc.keyboard_pvbus_s	0×1C060000	0×1C060FFF	0x00001000	^_auto_simple_buswidth_converter_25.isocket
vexpress_v9.lcdc.lcdc_pvbus_s	0x1C1F0000	0x1C1F0FFF	0x00001000	^_auto_simple_buswidth_converter_23.isocket
vexpress_v9.lcdc.mouse_pvbus_s	0x1C070000	0x1C070FFF	0x00001000	^ auto_simple_buswidth_converter_24.isocket

Add / Remov RTL Stubs Hybrid Adaptors & RTL Connectior





Editing a memory map

• a510_gic600_virtio_axi_hybrid already instantiates crouter as an interconnect Save to Catalog

Choose Starter Platform

Add / Remove

Confia / F^O

and Memory

- Easily add to memory map by multiselect of instances (initiators/targets) and ports
- "Validate" runs the Memory map rules checker
- **Reconfigure** generates the actual connections between router, targets and initiators





Save to Catalog

Add / Remove Virtual Models

Config / Port Binding

Add / Remove RTL Stubs

Hybrid Adaptors & RTL Connection

Debu

Create & Remove RTL Stubs

RTL Stub

RTL stub can be added using "Add Stub" button in early phase of development, when specific RTL IP is not integrated in design

- Helium supports to add • stubbing those RTL accesses and continue with bring up
- Remove the stubs when • RTL IP is up in design and allow accesses to reach to IP

👔 Problems 📮 Console 🔲 Men	nory Map 🛿							- 0		Click "Add Stub" button to create a stub in memory man fill in name
Memory Map						1	🖻 🗘 🗙 🖇	X +	6	start and end address.
type filter text								Ø		
💵 Port	IIII Base	Address	IIII End Addres	is Si	ize	🖬 Offset	•📽 Details			Click on this button to validate that
 hybrid_base.virtio_b.pvbus hybrid_base.virtio_c.pvbus hybrid_base.virtiop9.pvbus 	0X146400 0X146500 0X146600	00 00 00	0X1464FFFF 0X1465FFFF 0X1466FFFF	0> 0> 0>	<00010000 <00010000 <00010000		^_auto_simple ^_auto_simple ^ auto_simple	_buswidth _buswidth _buswidth		stub address is not overlapping with any other address
Stub_ddrc	0X147000	00	0X1470FFFF	0>	K00010000		Stub, DMI, Allo	Mem		
Problems 🖳 Console	∎ Memory Map 🛛		ld Range				🐔 🖃 🗘 🗙	• •		the stub addresses used in the memory map will need to be removed. After Stub removed
Memory Map		○ Ad	ld Stub				X (3 🖻 🕅	• 🎝 🕂		removed. After Stub removal
type filter text			Mem		1	1	1	-83		corresponding RTL IP
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>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>>	vbus 0X1	DMI			0X00010000	0	^_auto_simple_	buswidth_c	c	
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2 Peripherals	Masters								/	
SInterconnect hybrid_b	ase.ps_router							•		



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Helium Hybrid Adapters

 The Helium model catalog provides interface components (i.e. Hybrid Adaptors) to enable connections between:

Choose Starter Platform

Save to Catalog Add / Remove Virtual Models Parameter Config / Port Binding







ybrid Adapt & RTL Connection

Add / Rem RTL Stut

and Memory

Helium Hybrid Adapters

CPU Adapters

- Virtualize RTL cpu, pin-compatible with ARM FM core, connects seamlessly to RTL cpu wrapper using fast GFIFO communication channel
- GIC Adapters
 - Virtualize RTL GIC, pin-compatible with ARM FM GIC, connects seamlessly to RTL GIC wrapper using fast GFIFO communication channel
- ٠ Smart memory
 - Enables fast, concurrent, transparent view of memory to both virtual and RTL ٠ masters
- Bus Protocol Adapters (AXI, ACE, AHB, CHI)
 - Address RTL IP from virtual master, and vice versa, seamlessly connects with AVIPs
- Base Signal Adapters
 - Low level signal adapters for custom signal connection from TLM to RTL (sc signal tlm2rtl, sc signal rtl2tlm)

Search & Add virtual adapters for CPU and interrupt controller, Smart Memory OR Continue using from ref platform example and customize it based on need.

🗄 Catalog Browser 🖾 Project Explorer

Add / Remo

RTI Stub

type filter text

Parameter Config / Port Binding

Save to Catalog

Choose Starter Platform

Add / Remove

🗢 📑 Helium Model Catalog

- ♦ ⊕ example
- interconnect
- Interface
- memory
- peripheral
- platform
- - ARMCortexA35_rtlcpu_adapter
 - ARMCortexM7CT rtlcpu adapter
 - ARMCortexR8 rtlcpu adapter
 - ARMDynamIQ rtlcpu adapter
 - ARMTheodulDynamiQ rtlcpu adapter
 - ARMv8_rtlcpu_adapter
 - ace passive rtl2tlm
 - D 🖪 ace rtl2tlm
 - ▷ 🖪 ace tlm2rtl
 - ▷ 🖪 ahb rtl2tim
 - ▶ 🖪 ahb tlm2rtl
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 - Chi_a_tlm2rtl
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 - chi tlm2rtl



transactor gic400 bridge

vdefault

- gic400_bridge
- 🕶 🖴 gic500_mgr
 - ▼
 vdefault
- ▼ ▲ gic600 bridge
 - ▼ vdefault
 - gic600 bridge
- a gic600 mgr
 - ▼
 vdefault
 - gic600 mgr
- smart_memory

🔻 📸 Helium Model Catalog

➡ ☆ cadence com 🔻 🌐 transactor

 vdefault - smart_memory<32> smart_memory_32

vdefault - smart_memory<64>

- smart memory 64 vproxy - smart_memory_proxy<32>
- smart memory proxy 32 vproxy - smart_memory_proxy<64>
 - smart_memory_proxy_64

brid Adapto

& RTL

Connecti

- gic500 mgr

Configure RTL path in each Hybrid Adapter

Choose Starter Platform

Save to Catalog Add / Remove Virtual Models Rewire Interrup and Memory Map

Config / Port Binding Add / Rem RTL Stub

- Configure rtl_path parameter -
 - Of each hybrid adapter to connect to appropriate hierarchy in RTL design

Design Editor				Filter with "rtl_path"
rtl_path		•		
Name	Туре	Value	Details	
vexpress_v9	vexpress_v9			
 gic600_bridge_inst Parameters (8) 	gic600_bridge			Provide the hierarchical path of RTL side of Adaptor
	std::string axi_rtl2tlm	soc_rtl_top.gic600_mgr	Specify the hierarchical path of RTL ins	
 rtl_path rtlcpu_adapter Parameters (4) 	std::string ARMTheodulDynamIQ_rtlcpu_adapter	soc_rtl_top.gic600_mgr.axis_bfm	Set the AVIP BFM RTL instance hierarch	
	std::string axi_tlm2rtl	soc_rtl_top.cpu_subsystem.cpu_sig_mgr	Set path of RTL cpu adapter in RTL hier	
	std::string smart_memory<32>	soc_rtl_top.cpu_subsystem.axim_bfm	Set the AVIP BFM RTL instance hierarch	
rtl_path	std::string	soc_rtl_top.sm_mem_array	Set path of smart memory core in RTL	

lybrid Adapton & RTL Connection





CPU Wrapper Connections in Example SoC Hybrid

Save to Catalog

Choose Starter Platform

Add / Remove Virtual Models



Parameter Config / Port Binding Rewire Interrup and Memory Map

Add / Remove RTL Stubs Hybrid Adaptors & RTL Connection

RTL Side changes



Platform Build Options – Hybrid Platform

Choose Starter Platform

Save to Catalog Add / Remove Virtual Models Config / Port Binding

- Click on Project -> Configure Platform Build Options
- Add the specific build options required for Platforms
- Build Configuration
 - 'Palladium Hybrid' PZ1
 - 'Xcelium Hybrid' Simulation
 - 'Protium X1 Hybrid' Protium
- Skip RTL Build
 - If compiling RTL Snapshot separately Provide the path of *RTL Snapshot*

O Platform Ass	embly Build Settings <@sv07pd07>	⊙ ⊙
Clean Before Buil	ding 🕐	
f hybrid_elab.f -L` he global_verbosity_log	liumlib` /releasecatalog/cadence.com/util/global_verbosity_logger/vdefault/lib/release.20.0 jger -scNoDestructorsInElab	03/64bit -
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Hybrid daptors & RTL Connection

RTL Side

Add / Remove RTL Stubs





Debug

Run the Linux Demo - a510_gic600_virtio_axi_hybrid Platform

Add / Remove Virtual Models and Memory Map

Config / Port Binding Add / Remov RTL Stubs

Save to Catalog

Choose Starter Platforn

PalladiumZ1 Verification Computing Platform - xeDebug	×	l 📲 *new_platform_a	510 🛙			
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Sim Host: hsv-sc47 🛃 🖌 Board: 👘 IBoard:	1	0.469186 2.138247	581.802 udhcpc; scarced, v1.27	er er		
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	S Interconnect vexp	ress v9.ps router				



Hybrid daptors & RTL Connection

RTL Side changes



Questions



